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Carbon Nanotube Thin Film Transistor on Flexible Substrate and Its Applications as Switches in a Phase Shifter for a Flexible Phased-Array Antenna

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Carbon Nanotube Thin Film Transistor on Flexible Substrate and Its Applications as Switches in a Phase Shifter for a Flexible Phased-Array Antenna

by

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Dedication

To my Father

and to

my daughter

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Carbon Nanotube Thin Film Transistor on Flexible Substrate and Its Applications as Switches in a Phase Shifter for a Flexible Phased-Array Antenna

Daniel Thanh Khac Pham, PhD

The University of Texas at Austin, 2010

Supervisor: Ray T. Chen

In this dissertation, a carbon nanotube thin-film transistor is fabricated on a flexible substrate. Combined printing and stamping techniques are used for the fabrication. An ink-jet printing technique is used to form the gate, source, and drain electrodes as well as the dielectric layer. A self aligned carbon nanotube (CNT) thin film is formed by using a new modified dip coat technique before being transferred to the device substrate. This novel modified dip-coat technique utilizes the capillary effect of a liquid solution rising between gaps to coat CNT solution on a large area of the substrate while consuming minimal CNT solution. Several key solutions are addressed to solve the fabrication problems. (1) The source/drain contact with the CNT channel is developed by using droplets of silver ink printed on the source/drain areas prior to applying CNT thin. The wet silver ink droplets allow the silver to "wet" the CNT thin-film area and enable good contact with the source and drain contact after annealing. (2) A passivation layer to protect the device channel is developed by bonding a thin Kapton film on top of the device channel. This thin Kapton film is also used as the media for transferring the aligned CNT thin-film on the device substrate. Using this technique, printing the

passivation layer can be avoided, and it prevents the inter-diffusion of the liquid dielectric into the CNT porous thin-film. (3) A simple and cost effective technique to form multilayer metal interconnections on flexible substrate is developed and demonstrated. Contact vias are formed on the second substrate prior bonding on the first substrate. Ink-jet printing is used to fill the silver ink into the via structure. The printed silver ink penetrates through the vias to contact with the contact pads on the on the bottom layer, followed by an anneal process. High drain current of 0.476mA was obtained when V_G= -3V and source-drain voltage (V_{DS}) was -1.5V. A bending test was performed on the CNT TFT showing less than a 10% variation in performance. A bending test was also performed on via structures, which yielded less than a 5% change in resistance.

The developed CNT TFT is used to form a switch in a phase shifter for a flexible phased-array antenna (PAA). Four element 1-dimensional and 2-dimensional phased-array antennae are fabricated and characterized. Multilayer metal interconnects were used to make a complete PAA system. For a 2-bit 1x4 PAA system, by controlling the ON/OFF states of the transistors, beam steering of a 5.3GHz signal from 0^o to -27^o has been demonstrated. The antenna system also shows good stability and tolerance under different bending radii of curvature. A 2-bit 2x2 PAA system was also fabricated and demonstrated. Two dimensional beam steering of a 5.2GHz signal at an angle of $\theta=20.7^o$ and $\phi=45^o$ has been demonstrated. The total efficiency of the 1-dimensional and 2-dimensional PAA systems are 42% and 46%, respectively.

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Chapter 1: Introduction

I. Survey of carbon nanotube transistor development

Carbon has been used for centuries; however, many new crystalline forms of carbon have only recently been experimentally discovered over the last few decades. One of these new forms is the carbon-nanotube (CNT). Since its discovery, carbon nanotube has been gaining exponential interest, evident in the number of research articles published over the past decade. Figure 1 shows the publications and patent applications for carbon nanotube in recent years [1]. There has been a significant progress in understanding the fundamental properties and exploring possible engineering applications. CNT field-effect transistor (CNT-FET) and thin-film transistor (TFT) have been fabricated and characterized. Selected CNT-FET and CNT-TFT results are discussed below in this survey.

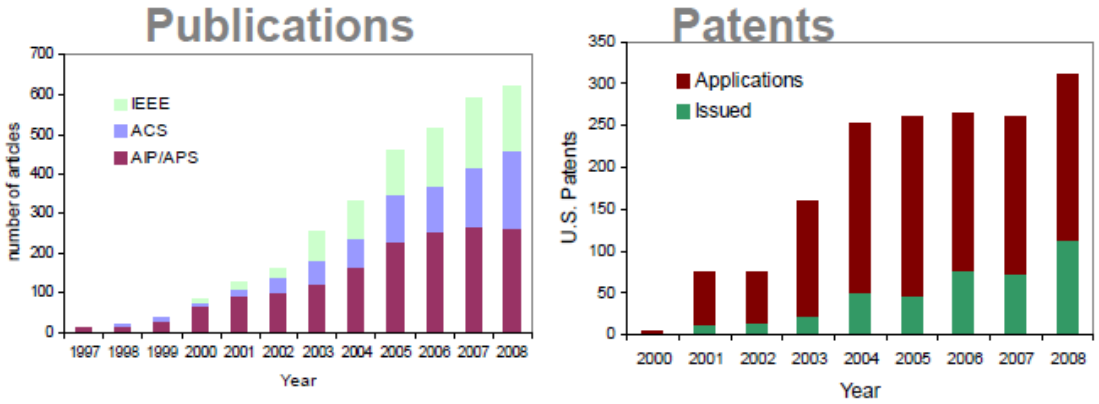


Figure 1: Publications and patent applications for carbon nanotube [1].

a. Lesson learnt from how to make CNT transistor – source and drain contact

Until now, most of the CNT research work has been mostly done on a silicon substrate. Beginning with the results from IBM, they demonstrated the first CNT-FET as shown in Figure 2 [2-4]. In these reports, back-gated CNT-FET structures were used. In the first device, high contact resistance (>1MΩ) was observed due to the CNT lying on top of the source and drain metal contact areas which could cause the scattering of the current at high drain voltage and high contact resistance.

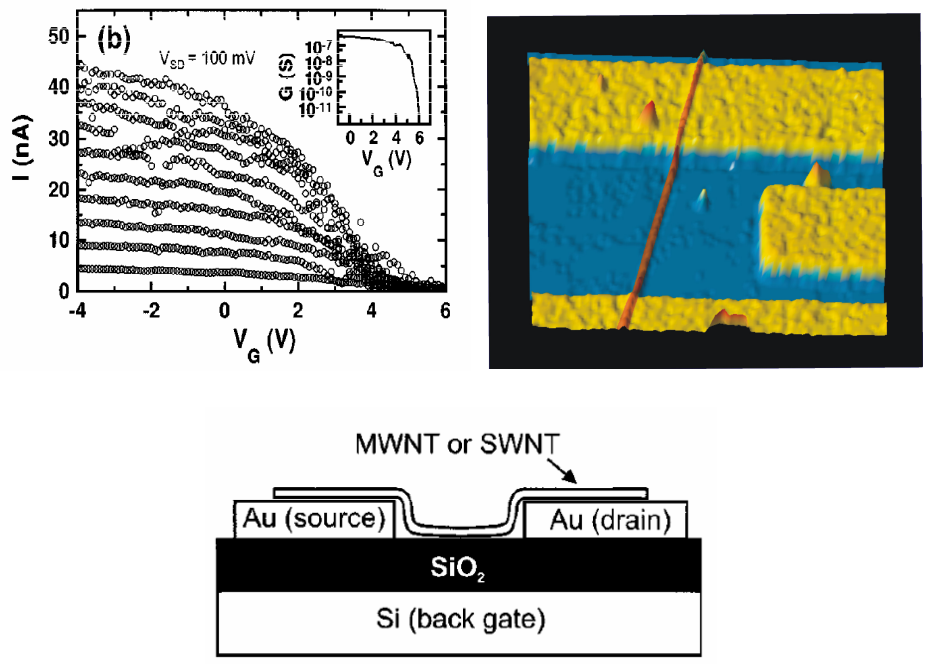


Figure 2: Martel et. al. (IBM) showed first CNT-FET published in Appl. Phys. Lett. (1998). Back gate device structure is used with CNT lies on top of the source drain contacts. The device showed high contact resistance (>1MΩ) [2].

The later results show better contact resistance since source and drain metal contacts were deposited on the CNT. From these reports, it can be observed that CNT-

FET works even when it lies on top of the source drain electrodes; however, better device performance is observed when source and drain electrodes are in contact with the CNTs (Figure 3).

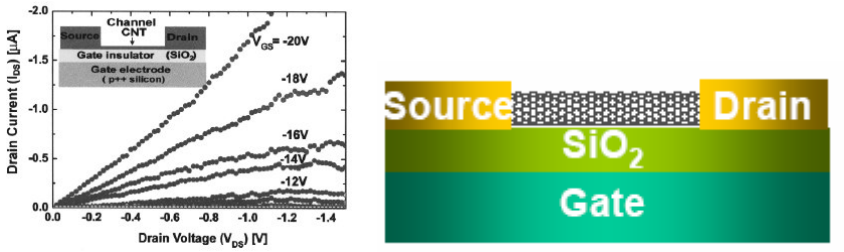


Figure 3: Avouris et. al. (IBM) published on Proc. IEEE (2003). Five year later, CNT device showed lower contact resistance (~30kΩ) [3]. In this device, source drain metal is deposited on the CNT channel.

Subsequent work performed by various groups have shown much better results using different kinds of metals for better contact, such as top and back-gate (electrostatic doping) [5], source drain doping [6], and even achieving ballistic transport (Lc <100nm) with Ohmic contact and self-aligned source drain structure [7]. These results, however, were achieved using a single CNT as the device channel, which is good for material investigation but impractical for most applications due to the small drive current (μA).

From the above CNT transistor development work, it is understood that the transistor works even when the CNT just lies on top of the source and drain metal contact areas. Better device performance is observed when the metal is deposited on the CNT for better contact resistance.

b. Aligned CNT

To achieve high performance device, a perfectly aligned array of single-walled CNT was reported [8-10] as shown in Figure 4 [8]. A chemical vapor deposition technique was used to grow the CNTs. More than 99.9% CNTs perfectly aligned to each other (within <0.01^{o}) using the chemical vapor deposition process. The CNT density was around ~10SWCNTs μm^{-1}, with average diameters of ~1nm and lengths up to 300μm. Due to the presence of metallic CNTs, the Ion/Ioff ratio was quite low.

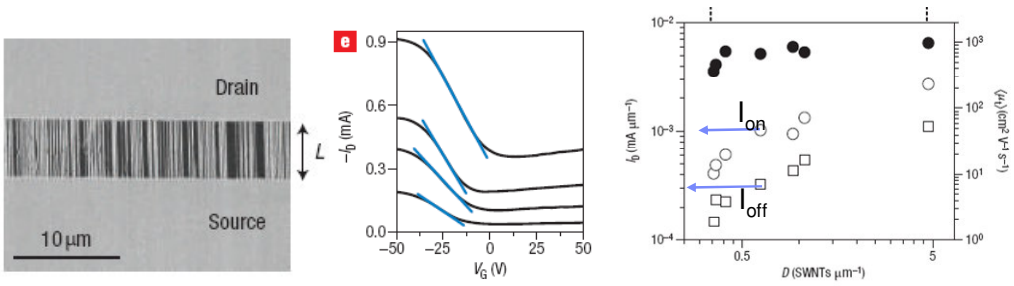


Figure 4: Kang et al. showed perfectly aligned array of SWCNT-FET channel [8].

An electrical breakdown process was used to eliminate the metallic transport pathways due to the metallic CNTs. This technique produced an increased Ion/Ioff ratio of the device as shown in Figure 5.

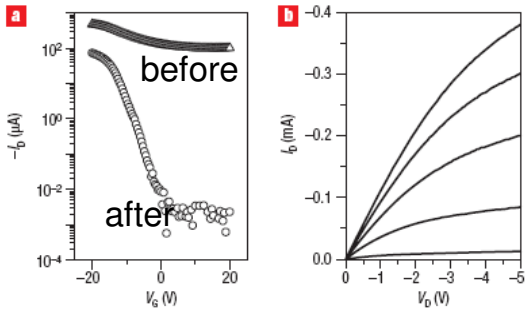
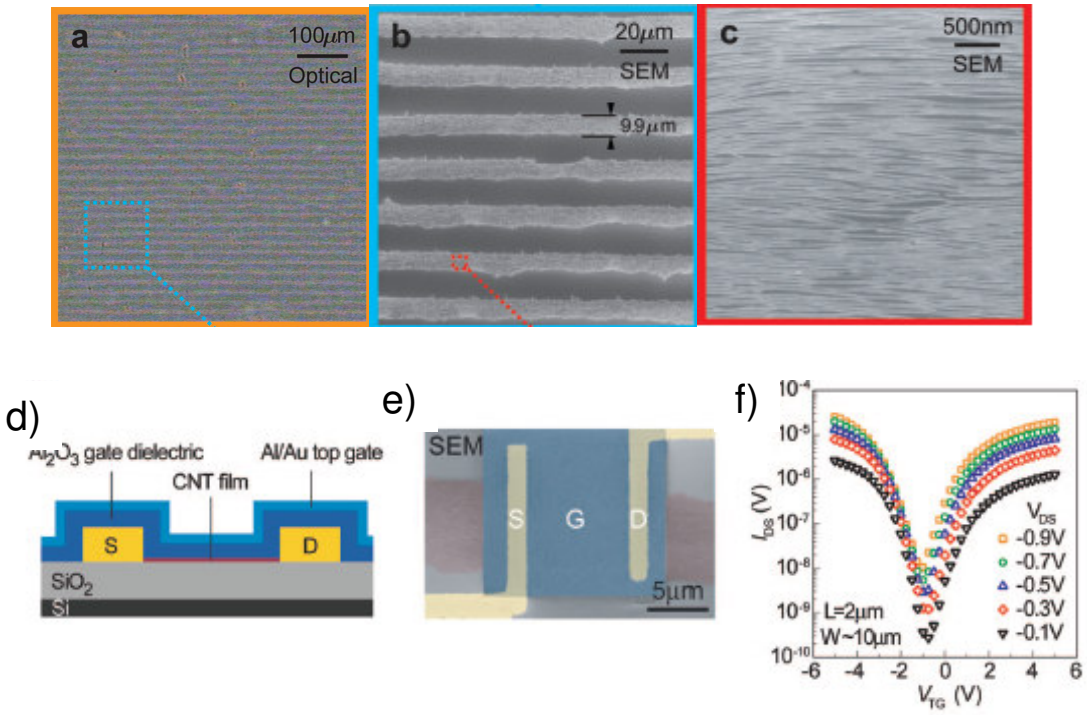


Figure 5: Electrical breakdown process eliminates the metallic transport pathway from source to drain and enhances the performance of the device [8].

Recently, a paper published by IBM on American Chemical Society-Nano Magazine [10] shows a simple technique to form self-aligned CNTs thin film by using the dip-coat technique. Self-aligned CNTs can be seen on the water contact line, as shown in Figure 6. From the publication, the device was formed on silicon substrate with a top-gated integration approach. As expected for CNT-FETs, ambipolar I-V behavior was observed. The Ion/Ioff ratio varied depending on the channel length. The channel length ranged from 0.5-10x of the average CNT length (~1μm). At the shortest channel length, high ON-state conductance was observed, but the device suffered from weak switching, reflected by its low Ion/Ioff ratio (less than 10).



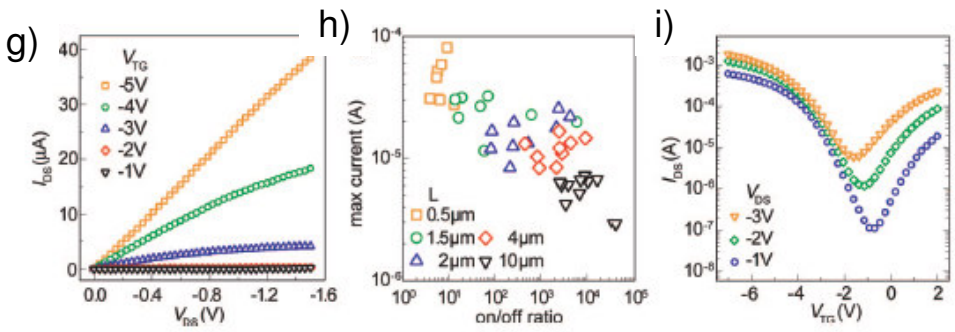


Figure 6: (a,b,c) SEM picture of self-aligned CNT and electrical data from IBM, (d,e) schematic and SEM image of the device, (f,g,h,i) electrical data of self-aligned CNT transistor [10].

Therefore, from the above we learn that CNT transistors made from single tube cannot be used for any practical application due to its low drive current. To improve the device drive current, multiple CNTs are needed on the device channel. Aligned CNTs on the device channel can provide the optimal drive current needed.

c. CNT transistor on flexible substrate

In reference [11], after forming aligned CNT transistor on silicon substrate, the perfectly aligned CNT transistors are transferred onto a poly(ethylene terephthalate) (PET) substrate as shown in Figure 7. The device contained aligned CNT density of 3SWCNTs □m^{-1} and used polyimide (1.6□m) and indium tin oxide (ITO) (150μm) as the gate dielectric and gate electrode, respectively. The mobility calculated in the linear regime was ~480$cm^2V^{-1}s^{-1}$. The device on flexible substrate was also subjected to bending tests as shown in the inset graph. Bending down to radius of curvature of 0.4cm

was performed. At such a high value of strain, the device failed due to fracturing of the gate electrode ITO.

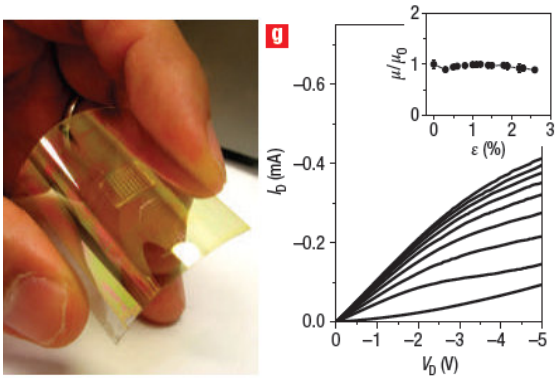


Figure 7: Perfectly aligned CNT-FET on flexible substrate transferred from silicon wafer. Id vs. Vd curve with the inset showing the normalized mobility as the function of bending induced strain (ε) [11].

Forming CNT-TFT (based on networks of SWCNTs) on flexible substrates has been of great interest for a lot of researchers around the world [11-14,16]. However, to achieve the device that is practical for any applications, high density of CNTs, with reduced or totally eliminated metallic CNTs or their conducting paths between source and drain electrodes are needed. Pimparkar et. al. [9] showed experimental and simulation data that by "striping" the CNTs channel into smaller segments, the Ion/Ioff ratio can be improved since the "striping" breaks the conducting paths of metallic CNTs, as show in Figure 8.

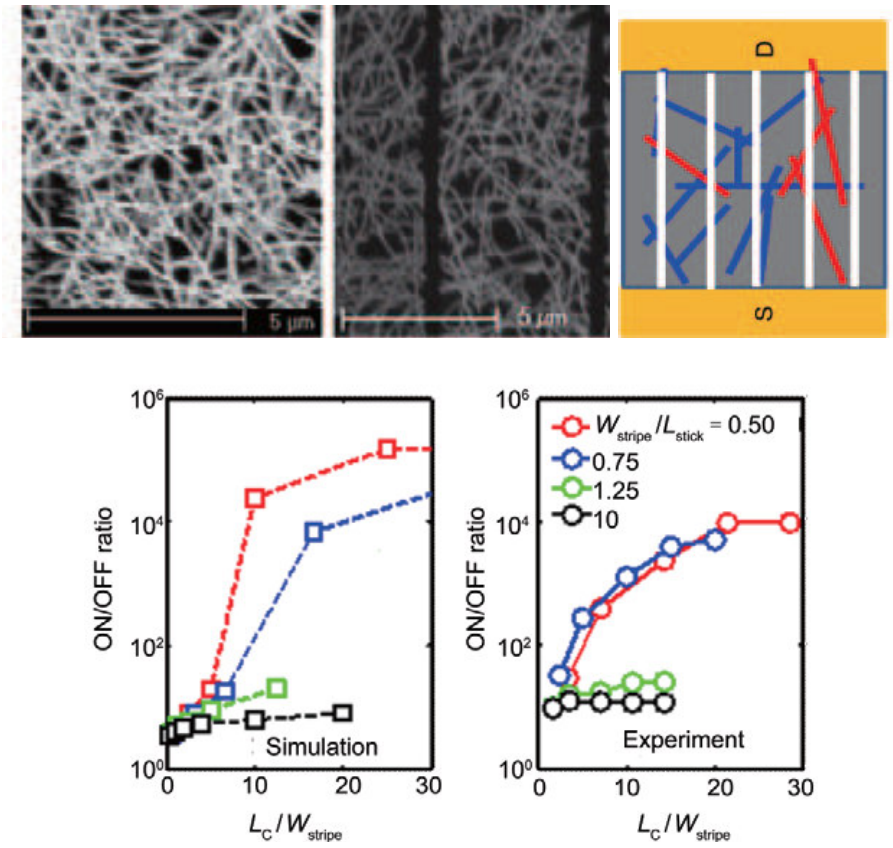


Figure 8: By "striping" the CNTs channel into small segments, the conducting paths are cut-off, yielding higher Ion/Ioff ratio. Lc: channel length; Lstick: stick length [9].

Recently, highly pure semiconducting CNTs are formed and commercially available with Nanointegris, Inc which is a company based in IL. Using a combination of surfactants, where different surfactants bind selectively with different CNT types, semiconductor and metallic CNTs can be separated from each other. Currently, 99% pure of either CNT type is available commercially. Several publications [10,15,16] have shown interesting results using these high purity CNTs. This highly pure semiconducting CNT can be applied on flexible substrate to form several different device applications.

In summary, recent results from CNT-FETs and CNT-TFTs devices have shown great progress in improving performance in the last decade. In general, high density of semiconductor CNTs along with reduction or elimination of the conducting paths of metallic CNTs are needed in order to obtain good device performance for any application, either on silicon or on flexible substrates.

II. Dissertation overview

This dissertation is organized as following:

Chapter 2 describes the integration of CNT-TFT on flexible substrate including novelty approaches to solve the source and drain contact issue with CNT channel and a method to passivate the CNT channel. In this chapter, a self-aligned CNT thin-film technique is described. Device results showing higher drive current from self-aligned CNTs channel compared to random CNTs are discussed. Bending test on CNT TFT is performed and less than 10% performance variation is demonstrated.

Chapter 3 describes techniques to form random and aligned CNT thin film. A novel technique has also developed to provide self-aligned CNT thin film but using less CNT solution.

Chapter 4 describes the fabrication process for CNT TFT on flexible substrate. Introduction to ink-jet printing and detail fabrication steps are presented.

Chapter 5 shows the fabrication technique to form multilayer metal interconnect for flexible circuit. Bending test on contact via and reliability test on via chain structure are discussed.

Chapter 6 describes the 1-D and 2-D phased-array antenna design and fabrication process. Far-field radiation results of flat and bending antenna system are reported. Simulation model and data for the phased-array antenna system are discussed.

In the final chapter, chapter 7, the results are summarized and future directions are discussed.

In Appendix A, an overview of simulation works for CNT transistor have been reported. Then, the model and simulation approach used for this research is discussed. Other Appendixes contains simulation codes for PAA design and simulation data.

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Chapter 2: Carbon nanotube thin-film transistor

I. Introduction

As mentioned in Chapter 1, the first CNT transistor reported by group at IBM used a bottom gate structure [1]. A CNT transistor consists of a single CNT lying on top of the source, drain and gate electrodes. The bottom gate structure is used due to its simplicity. The device, however, has a high contact resistance. Later, an improved CNT transistor was made with source drain metal deposited on the CNT [2]. Even better device performance is observed when a top gate structure is used for the CNT transistor [3]. Top gate integration for a CNT transistor is normally used when it is formed by using semiconductor processing where the materials are deposited by semiconductor equipment. These materials are deposited from the gas phase; therefore, the films are deposited uniformly. In this research, an ink-jet printing technique is used to deposit metal (silver) and dielectric (spin-on glass or photo resist). These materials are in liquid form and normally are hydrophilic on the flexible substrate to provide better film coverage. In this Chapter, novel techniques have been developed to provide solutions for CNT TFT on flexible substrates.

II. Carbon nanotube thin film transistor integration

Both bottom gate and top gate integration approaches are used in these experiments. There are advantages and disadvantages in the use of either approach. Depending on the printing technique, the integration needs to be adapted accordingly.

In this work, a printer from Dimatix [DMP 2800] is used. The ink droplet is dispensed from an ink cartridge with a nominal volume of 10pL. This ink droplet volume

is large and could cause the printed material to penetrate or diffuse into porous media. In Chapter 5, fabrication techniques using ink-jet printing will be discussed in detail.

For the printing technique, ink droplet size and liquid ink viscosity are very important parameters to choose in the integration, due to the advantages and disadvantages for each integration approach. Table 1 shows a comparison between these integrations.

Integration	Advantage	Disadvantage
Top gate	♦ CNT deposited first ♦ Dielectric and Gate electrode materials cover the CNT channel ♦ CNT channel has good contact with S/D metal printed on top of the channel plus annealing	♦Dielectric material diffuses between CNTs and separate them (also depending on printing technique) ♦ High thermal budget
Bottom Gate	♦ CNT channel deposited last. No interaction with dielectric and gate materials. ♦ Low thermal budget for CNT channel	♦ CNT channel has bad contact with S/D metal (solution identified) ♦ No passivation – CNT channel exposed to air (solution identified)

Table 1: Comparison between top and bottom gate integration method using printing technique.

After several experiments, the bottom gate approach was chosen for this research, mainly due to the printing technique compatibility. In order to overcome the

disadvantages of using the bottom gate integration approach, novel solutions have been created. The schematic of the bottom gate integration process flow used in this work is shown in Figure 9.

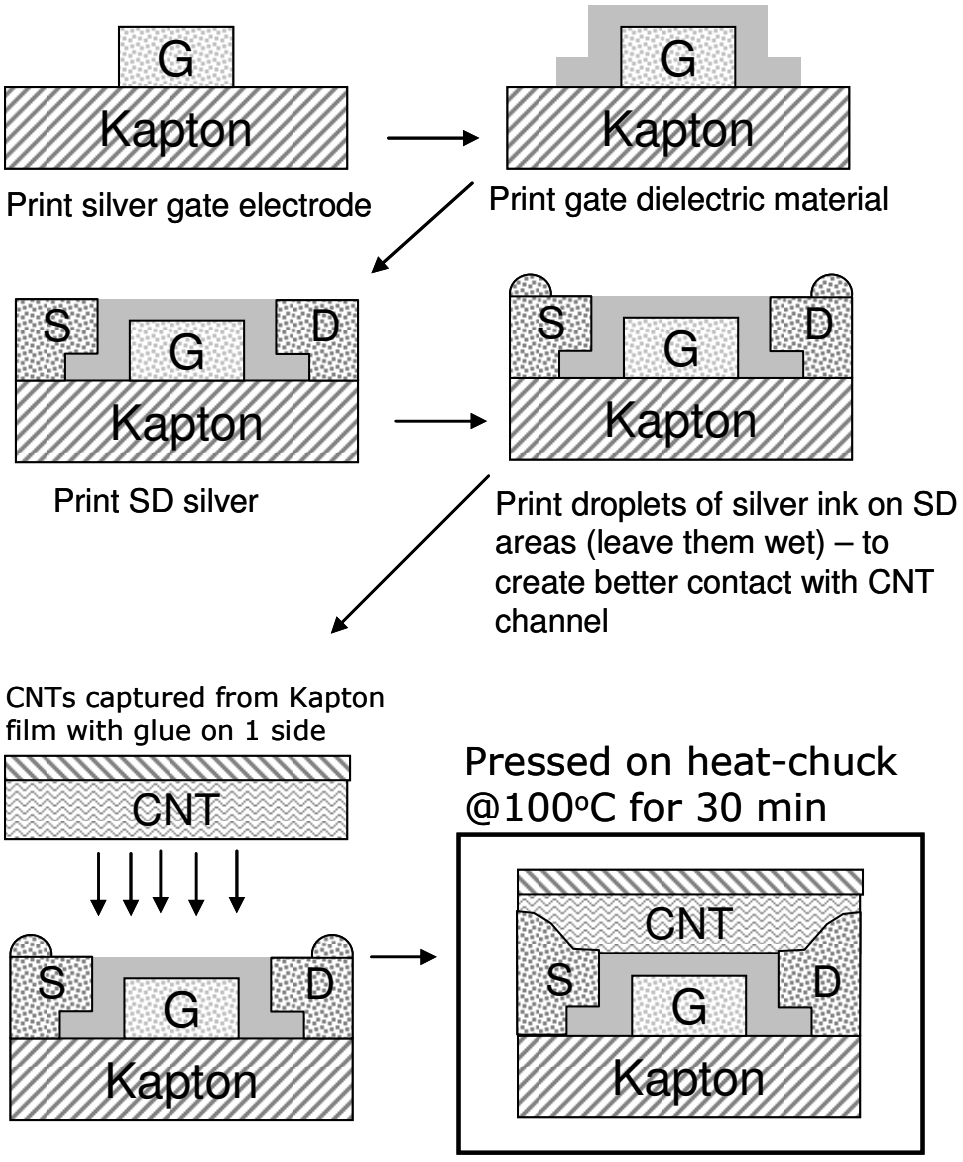


Figure 9: Bottom gate integration with novel source-drain contact and passivation layer for CNT channel. Wet silver ink droplets on source drain contact in step 4 provide good contact with CNT channel. Thin Kapton film with aligned CNT film is left on the device.

A Kapton Polyimide substrate with a thickness of 125μm is used. The gate electrode is first printed on the Kapton film using silver ink, followed by thermal annealing at 160^{o}C for 10 minutes. Spin-on-glass or photo resist is used as the dielectric material, which is also printed. Then, the source and drain regions are printed using the same silver ink as used for gate electrode and under the same annealing conditions. The device channel length is designed at 60μm and the width is 300μm (due to transmission line width). For the small structure, only one nozzle is used during the printing in order to maintain resolution. This printing technique is discussed in Chapter 5 for the fabrication process. Due to the clog-up issue of the printer cartridge and the buckling of CNT when printing, the CNT is deposited using a transfer process. The technique of such CNT thin film preparation is discussed in Chapter 3. In order to transfer the CNT thin-film onto the flexible Kapton polyimide substrate, another special Kapton substrate (with adhesive coating on one side), is used to lift the self-aligned CNT thin-film from the silicon substrate and lay it on top of the first substrate over the printed channel region. The Kapton with adhesive is left on the device in order to protect the CNT channel, thus acting like a passivation layer. This passivation layer provides a novel solution to solve the disadvantage of bottom gate integration discussed above. Due to ink droplet size and the viscosity of the printable material for Dimatix printer, normal passivation layers (such as dielectric material – spin-on glass or photo resist) cannot be used. The CNT film is a porous layer, thus the printed passivation materials will diffuse between CNTs and cause the CNT to separate from each other.

Prior to bonding these two layers, another novel technique has been developed to enhance the contact between CNT and source-drain areas. In this technique, droplets of silver ink are printed on the source and drain areas on the first substrate as shown in Figure 10. These wet silver ink droplets allow the silver liquid to "wet" the CNT thin-film area and enable good contact with the printed source and drain contact. In order to bond the two substrates, the device is annealed under pressure on a heated chuck at 100^{o}C for 30 minutes to enhance the bonding of the second Kapton substrate to the first substrate and to eliminate any air pockets. The annealing process is also discussed in Chapter 5. Upon bonding and annealing, the source-drain contact junction is formed into the CNT thin-film, thus providing a good contact with the entire thin film. Without using the wet silver droplets to enhance the contact, the ON current is very low ranging from a few nano to a few micro-amps.

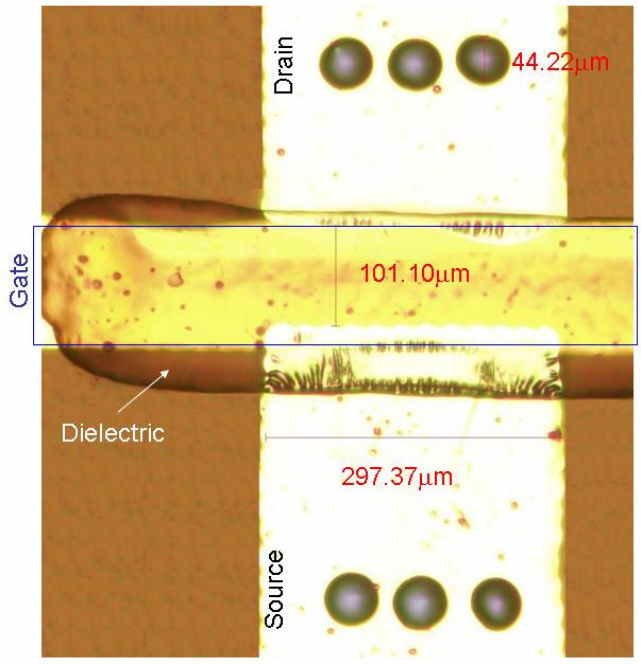


Figure 10: Wet silver droplets on source-drain areas before bonding with CNT thin-film.

In summary, novel solutions have overcome the disadvantages of using bottom gate integration in this work. This integration is chosen due to the liquid ink droplet size of the printing technique available for this research.

III. Carbon nanotube thin film transistor characterization

1. Electrical data from printing and applying ink droplet on the channel

In the early stages of this research, a CNT solution (solution number B96100) from Brewer Science was printed. As mentioned in Chapter 3, the CNT solution is printable; however, it is often clogs the cartridge. Testing samples with different layers of CNT from Brewer Science are formed to investigate the drain current versus number of CNT layers. The results show a small number of working test transistors. This could be because the CNT water solution forms a "fracture thin film" upon drying as discussed in Chapter 3. Figure 11 and 12 show picture and data of 25 CNT layers and full droplet results.

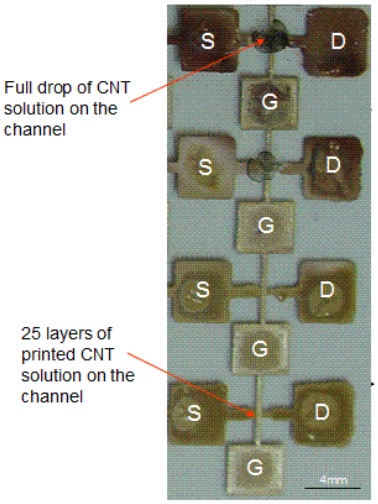
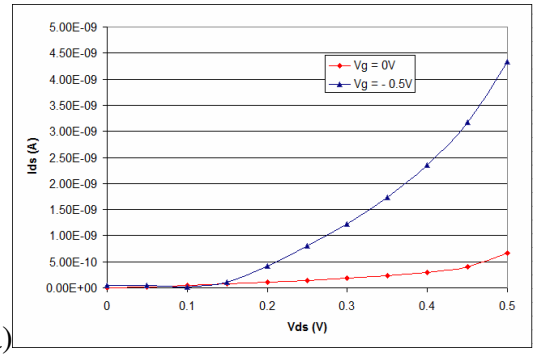


Figure 11: Different transistor samples consisting of varying amounts of CNT.

a) 

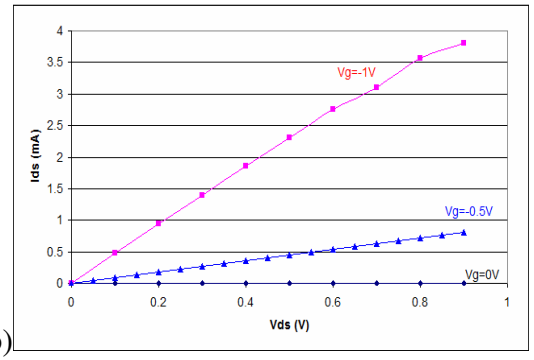
b) 

Figure 12: I-V characteristics of FET utilizing active layer formed using (a) 25 printed CNT layers, and (b) a droplet of CNT solution.

The technique of forming CNT channel by printing or droplet formation is unstable due to the "fractured" thin film formed and due to the clogging problem of the cartridge. Therefore, this technique is not employed for this research. Even though applying CNT droplet on the device channel or soaking the whole substrate into liquid CNT has been used in some reports [6,7] showing good CNT transistor device performance, these techniques are not considered for this research due to the hydrophobic surface property of Kapton substrate and the large phased-array antenna system to be built.

2. Electrical data from random carbon nanotube network

Data from the random CNT networks using the filtering technique (discussed in Chapter 3) with the CNT from NanoIntegris is shown in Figure 13. In the same figure, I-V plots from Nougaret et. al. [5] are also included, which show similar characteristics.

Both data are obtained from the same CNT material, and from the same technique of forming random CNT networks.

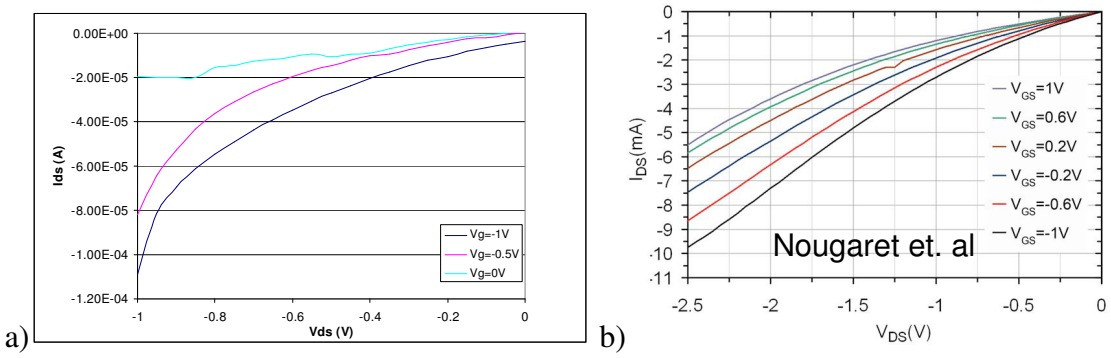


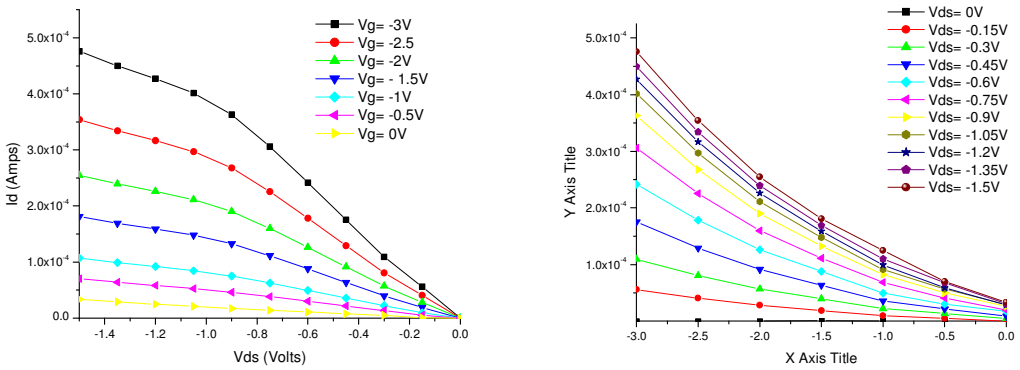
Figure 13: (a) I_D-V_{DS} using random CNT thin film by filtering technique and (b) from reference [5] using CNT solution from the same source.

The advantage of using this technique is the CNT density can be estimated from the solution concentration and the surface area of the filter. However, the CNT film is a random network of CNTs. If aligned CNT film can be made, then aligned CNT film as device channel will provide better device performance data, as shown in experimental and simulation data [7,10,11]. For that reason, the technique to form aligned CNT has been developed as discussed in Chapter 3 and electrical data is discussed below.

3. Electrical data from self-aligned carbon nanotube thin-film

Figures 14(a) and (b) show the measured I-V characteristics (I_D versus V_{DS}) of the self-aligned CNT-TFT as a function of different gate voltages (V_G). The transistor I-V characteristics are measured using a precision semiconductor parameter analyzer (Agilent 4156C). At a gate voltage of 0V gate, the device does not show pinch-off, most likely due

to a small number of metallic nanotubes in the channel. At V_G= -3V and source-drain voltage (V_{DS}) of -1.5V, a high drive current of 0.476mA is obtained, which is in good agreement with the high density and self-aligned nature of CNTs on the device channel (discussed in the simulation chapter – Chapter 4). As mentioned in Engel et al. [4], CNT-TFT can have I_{on}/I_{off} ratio as high as 10^5; however, any improvement for the on-state current will degrade the I_{on}/I_{off} ratio due to the increased number of metallic pathways between source and drain. In this work, the I_{on}/I_{off} ratio is around 20. Further optimization such as using an electrical burning off technique to eliminate metallic pathways will be discussed later in the chapter.



a) b)

Figure 14: (a) I-V characteristics (I_D versus V_{DS}) of the self-aligned CNT-TFT at different gate voltages, (b) I_D versus V_G of the self-aligned CNT-TFT.

Figure 15 shows I_{ON} and I_{OFF} values of several devices. In the beginning of the research, the V_{DS} is scaled back to -1V because previous devices (without passivation layer) were found to be unstable after high voltage test. Later, the voltage is set to -1.5V and shows stable I_{ON} current. The I_{ON}/I_{OFF} ratio is also improved as shown in Figure 16.

Further increasing the V_{DS} voltage causes unstable device, which might be due to the heat generated in the channel under high current (also discussed below).

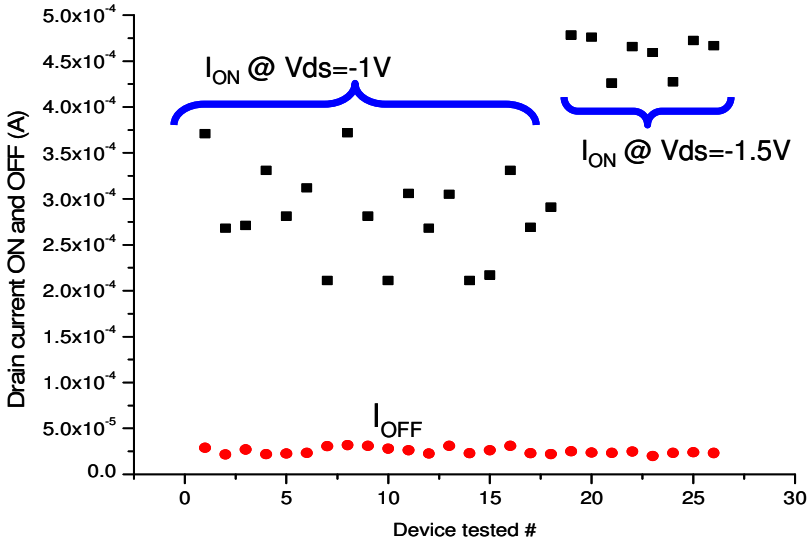


Figure 15: I_{ON} and I_{OFF} values of several devices tested at V_{DS}= -1V and -1.5V.

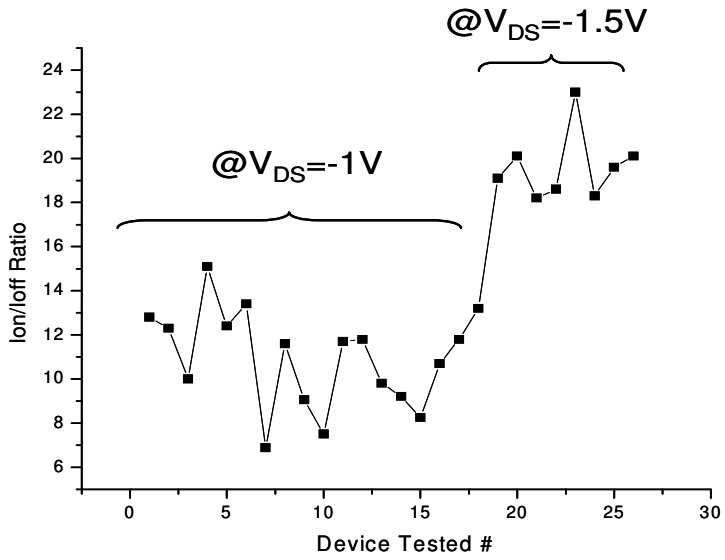


Figure 16: I_{ON}/I_{OFF} ratio of several devices tested at V_{DS}= -1V and -1.5V.

Aligned CNT thin film provides stable and higher device performance than other techniques discussed above. Similar result is reported by group at IBM using the same source of CNT and same CNT aligning technique [4]. Therefore, using aligned CNT thin film as the device channel is chosen as the processing choice due to these good results.

IV. Further work on carbon nanotube thin film transistor

1. Electrical breakdown of metallic pathway

To improve CNT TFT device Ion/Ioff ratio, electrical breakdown of metallic pathways from source to drain has previously been investigated [7-9]. In this technique, a large positive voltage is applied to the gate and a negative voltage is applied across source and drain. Since the CNT transistor is a p-MOS device, the large positive gate voltage turns off the p-type semiconducting CNT. The current going through metallic pathways breaks off the metallic CNTs after several sweeps. The voltage applied to gate or source drain needs to be selected carefully to minimize the degradation of the device channel. Long channel device may require large voltage to breakdown, although the exact relationship depends on many factors, including degree of heat sink to the electrodes [8].

Reported electrical breakdown of metallic pathways are performed on CNT transistor fabricated on silicon substrate and dielectric layers of silicon dioxide or high-k material (HfO_2). The silicon substrate provides a good heat sink to the device to prevent damage to the device channel, especially to the dielectric layer. Kapton substrate is not a good heat conducting layer. High channel current will cause damage on dielectric layer or

other material (such as polymer conducting material using as gate electrode). In the early stages of the research, I evaluated CNT TFT samples fabricated by Dr. Xuejun Lu's group at the University of Massachusetts - Lowell using Brewer Science CNT solution and using top gate integration with polymer material as dielectric layer and conducting polymer as gate electrode, air bubbles are observed on the device channel after electrical testing. When air bubbles were observed, attempting re-testing showed the devices to be shorted. Figure 17 shows microscope pictures of device having bubbles in the channel after electrical testing. These air bubbles are formed due to the heat generated in the device channel.

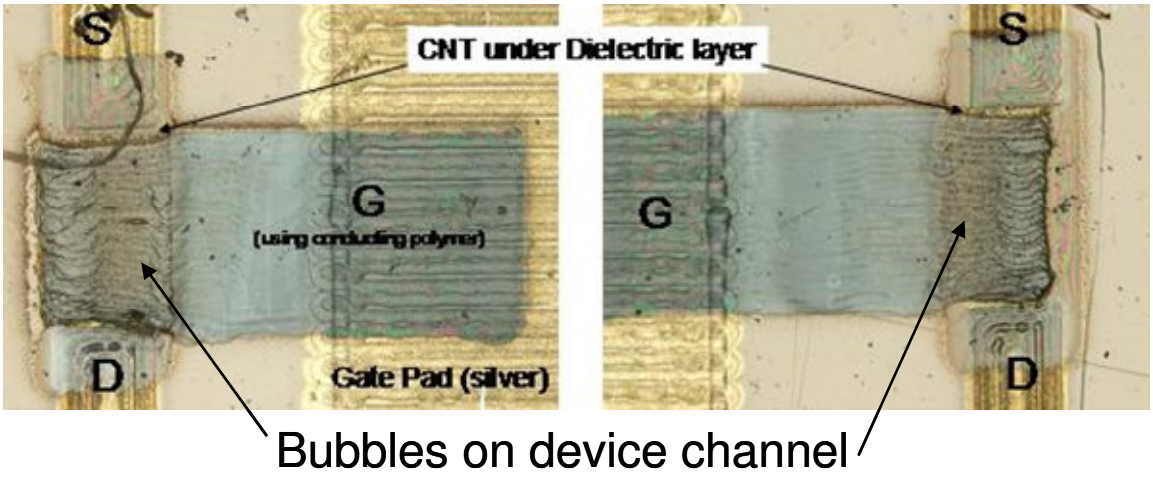


Figure 17: Microscope images of CNT transistor having bubbles on the device channel after electrical testing.

Two different electrical breakdown tests are performed for this research, constant voltage breakdown and short pulse voltage breakdown. These techniques are discussed below.

Constant gate voltage breakdown test:

From reference [7] and [8], the breakdown conditions are: Reference [7]: Gate voltage +20V, Source-drain: from 0V to negative up to 50V. Reference [8]: Gate voltage +20V and up to +50V. Source drain: negative voltage.

For this work, several attempts to sweep the device at positive gate voltage are conducted. The gate voltage is increased in positive direction starting from 0V with +2V increment. The source drain voltage is swept from 0 to -15V at each gate voltage and the device is re-tested to obtain Ion/Ioff ratio. It is observed that after the breakdown voltage test, the device is shorted. It indicates that this constant voltage test is not suitable for the device. The technique could not yield any result. Notice that the constant voltage breakdown conditions are different to the operating conditions of the CNT TFT. In electrical breakdown conditions, high positive gate voltages are applied to the gate to turn off the semiconductor tubes, while in normal operating conditions, negative and lower (absolute value) voltage are using for both gate and source drain.

Pulse gate voltage breakdown test:

Since constant gate voltage breakdown may cause damage to the gate dielectric layer, a pulse gate voltage breakdown test is developed. The voltage pulse width of 5ms, 25ms, 50ms, and 100ms are used for the experiment. The pulse period is kept at 1s to allow the channel to cool down after each voltage stress as shown in Figure 18. Same pulse width and pulse period are applied for gate and source-drain voltages. The pulse gate voltage is ramped from 0V to +50V, and the pulse source-drain voltage is also

ramped for each gate voltage from 0V to -15V. After each pulse voltage sweep, an I_d-V_g test is performed to see if there is any improvement in I_{ON}/I_{OFF} ratio.

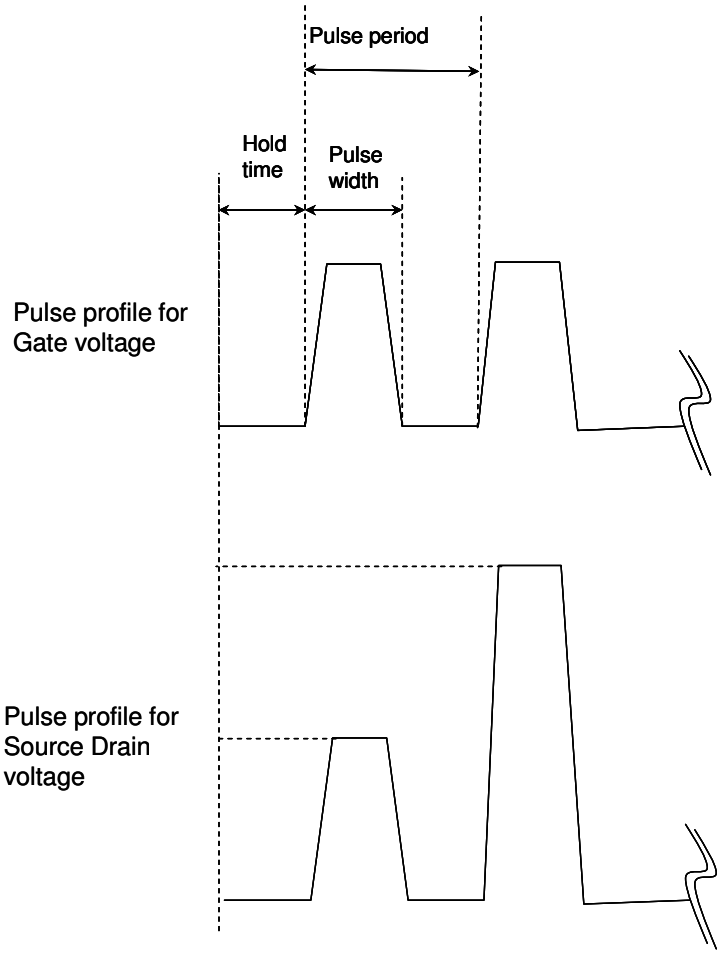


Figure 18: Schematic of pulse gate and source-drain voltage breakdown test.

Several different pulse widths are used: 5ms, 25ms, 50ms, and 100ms. The pulse period is kept at maximum 1s to allow cool down of the channel.

Figure 19 shows I-V characteristics results before and after pulse electrical breakdown test. The I_{ON}/I_{OFF} ratio is increased from 18 to 61. However, the drain current is degraded. The reduction in both on and off stage drain currents indicate that the metallic conduction paths are eliminated. This behavior has been also reported from

several publications [7-9]. Although the drain current is lower, such TFTs can be used in applications wherein high I_{ON}/I_{OFF} ratios are desired, such as in a phased array antenna circuit.

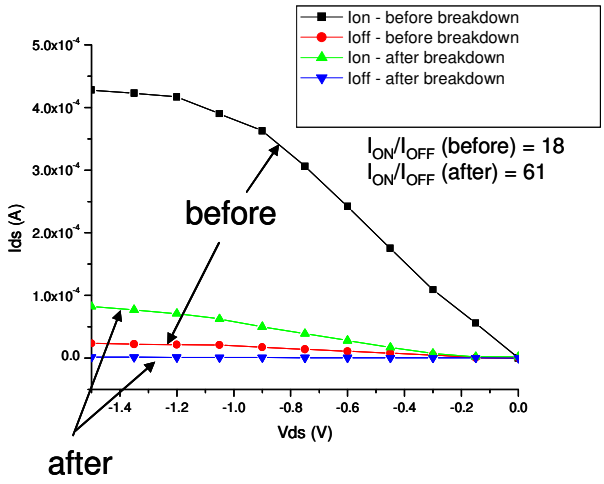


Figure 19: I_D-V_{DS} results of device before and after pulse electrical breakdown. The I_{ON}/I_{OFF} ratio is increased from 18 to 61.

2. Investigate CNT TFT with difference channel length

From simulation data in Appendix A, shorter channel length (shorter than 100μm) will increase the drain current without increasing the channel width (the channel width is limited by the antenna transmission line width of 300μm). Therefore, experiment to reduce device channel length for CNT TFT has been performed. As mentioned in Chapter 5, photoresist and spin-on glass droplets on Kapton substrate have the diameter of 150μm and 250μm, respectively. Large droplet on the Kapton substrate is due to the low viscosity and wettability of these materials. The large droplet diameters will cause the

resolution limit to print these materials become larger than silver ink. Also, the surfaces of these two materials are hydrophilic with silver ink. Surface hydrophobic will prevent silver ink to print smoothly on these materials (printed source drain defining the channel length).

Figure 20 shows the microscope pictures of the photoresist material printed on top of the gate structure. Single pass of photoresist has the dimension more than 3 times the width of the gate electrode (gate electrode is designed 60µm, actual measured as 92µm). Upon drying the photoresist, the surface of the photoresist line becomes hydrophobic. Due to these reasons, further scaling down the device channel device is limited. Therefore, working device in this research has the channel length range from ~100µm actual to ~200µm actual. With a narrow range of channel length that can be achieved but large variation in drain current, as shown in Figure 16, study of device performance versus channel length is limited by the fabrication process and materials.

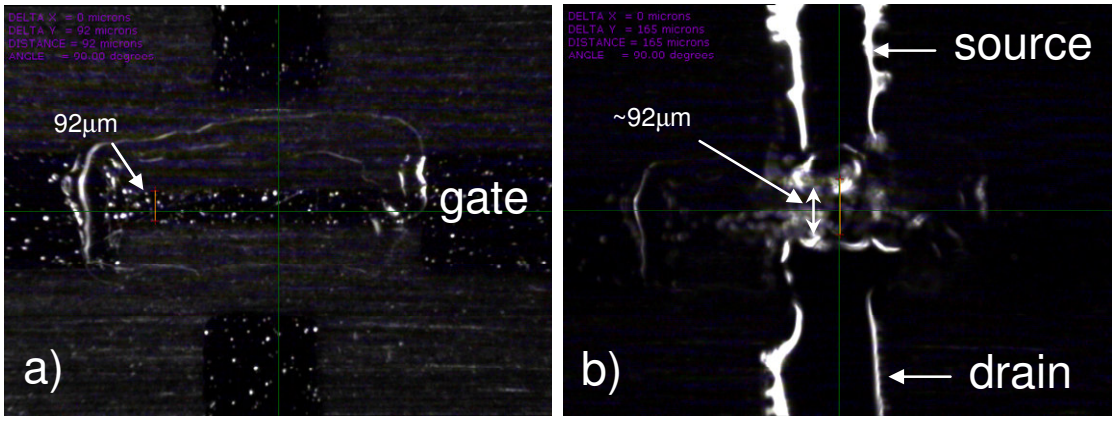


Figure 20: a) Printed photoresist spreads on device channel, b) Area surrounding the photoresist becomes hydrophobic, and it is hard to form small channel length on this hydrophobic surface.

3. Carbon nanotube thin film transistor bending test

Bending test experiment has been performed on CNT TFT. This test is required to evaluate the reliability of flexible circuits employing CNT TFTs under different bending conditions. Figure 21.a shows the picture of the bending test structures. Two different test structures are formed to evaluate the vertical and horizontal orientations of the transistor. Three different radii of curvature, 4.5mm, 3mm and 1.5mm, are used in this evaluation. Forward and backward bending tests are conducted as described in Figure 21.

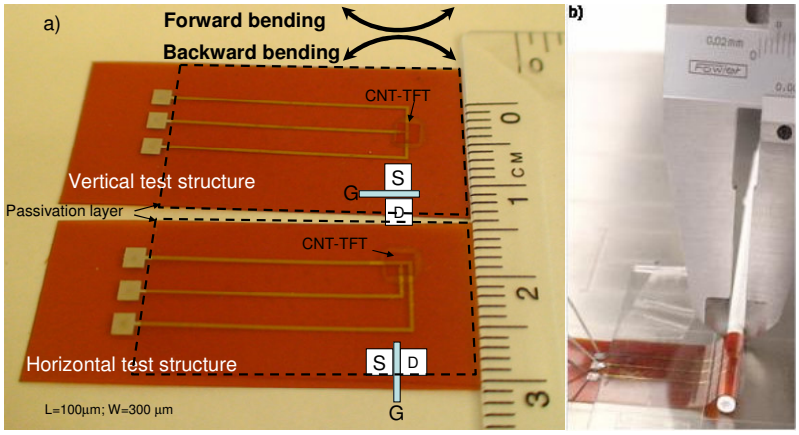


Figure 21: a) Bending test structure for vertical and horizontal devices, b) Device under backward bending test at 1.5mm radius of curvature.

Figure 22 shows the normalized drain current ($I_{D,test}$ / $I_{D,original}$) plotted against radius of curvature for the vertical test structure. In forward bending, a lower drain current is observed, with up to 10% change, while no significant drain current difference is observed in the backward bending case. Larger current changes for the vertical test structure can be attributed to the 300µm channel width of the testing device subjected to

the bending direction. Since the CNTs are captured by the thinner Kapton film that is bonded onto the thick Kapton substrate, forward bending may cause movement of the thin kapton film away from substrate, while in backward bending, it causes the thin Kapton film to press against the substrate.

Figure 23 shows drain current bending test data for horizontal test structures. Smaller changes in drain current are observed (less than 6%). For the horizontal test structure, the 100µm channel length of the device is placed in the bending direction. In the forward bending case, the shorter channel length causes a small increase in current, and in the backward bending case, the "stretched" channel length reduces the current (even though the thin top layer Kapton is pressed against the substrate).

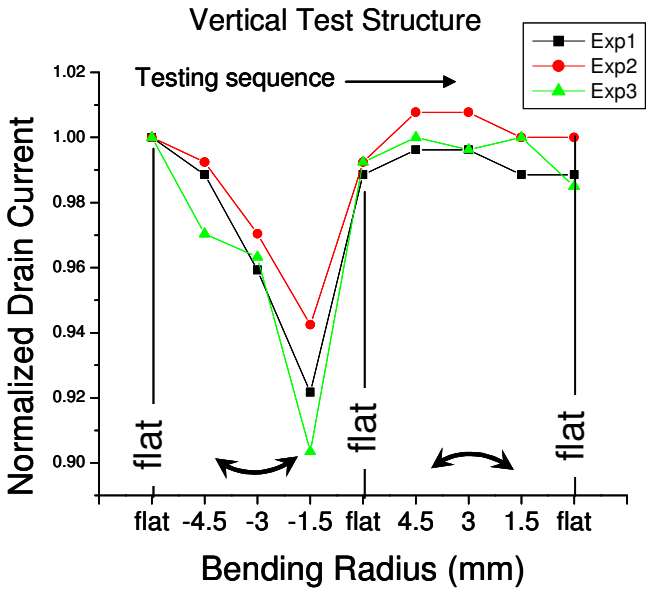


Figure 22: Bending test data for vertical test structure.

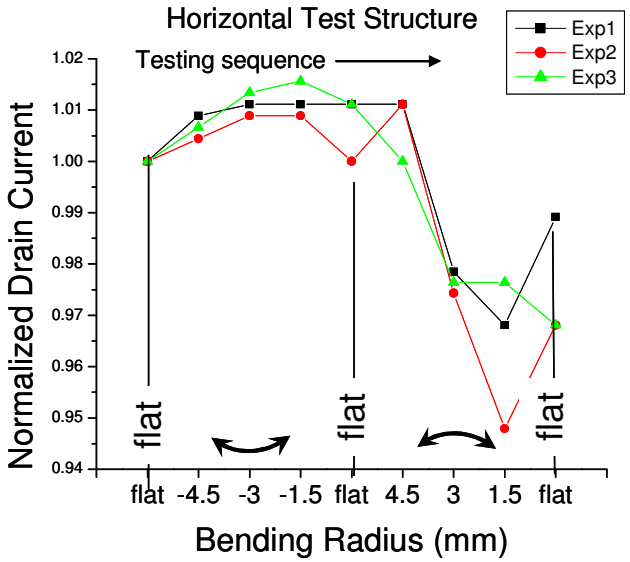


Figure 23: Bending test data for horizontal test structure.

In summary, self-aligned CNT TFT has been demonstrated using 99% pure semiconducting nanotube on flexible Kapton substrate. A novel source-drain contact is developed to enhance the contact with CNT channel. Passivation layer is also developed providing stable device performance. Bending test data show minimal changes (less than 10%) in their performance.

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Chapter 3: Carbon Nanotube Thin-Film Formation

I. Introduction

Commercial carbon nanotube inks are available for several different printers, even for personal copier [1,2]. Printed CNTs using off-the-shelf cartridges and printers are used as conducting material for several applications. Using conventional cartridges, CNT solution can be jetted out without clogging problem, as discussed in Chapter 5, using the Dimatix printer available for this research.

In this chapter, an alternate technique has been developed to form CNT thin film providing stable material to form CNT TFT device.

II. Carbon nanotube thin film formation

Two different CNT thin films have been made for this research - a) random CNT network thin film and b) aligned CNT thin film. In both techniques, 99% pure semiconducting CNT material from Nanointegris, Inc and 98% pure semiconducting CNT from Brewer Science are used. The CNT solution from Nanointegris contains a surfactant. Techniques of making them are discussed below.

1. Random CNT network thin film

Using a filtering technique, random surfactant-free thin film CNT can be formed on the Kapton substrate using the following process:

a. The diluted CNT solution is passed through a Mixed Cellulose Ester (MCE) nanopore filter, as shown in Figure 24(a). Due to the nano pores, only surfactant and water can pass through the filter. Thus, a thin-film of nanotubes will accumulate on the filter's inner surface. A picture of MCE film after passing CNT solution through it is shown in Figure 24(b).

b. Once the desired volume of CNT solution has been filtered, the CNT film is set aside for approximately 15 minutes and then rinsed gently with ~1 mL of 2-propanol followed by ~30 mL of water. The film is allowed to set again for 15 minutes

c. The nanotube-coated MCE filter is briefly dipped in ethanol, and using gentle pressure, the filter film is pressed face-down against the Kapton substrate, as shown in Figure 24(c).

d. Immediately, the substrate/filter is suspended horizontally over a bath of boiling acetone (suspend filter-side up, approximately 2" above the liquid.) The acetone vapors will gradually dissolve the MCE filter. It is let to sit until the MCE filter is no longer visible (usually about 1 hour).

e. The substrate is placed in a stirred bath of liquid acetone for 15 minutes to remove the remaining MCE residue and then immediately transferred to a stirred bath of methanol for an additional 15 minutes.

f. The CNT film is gently dried with compressed air.

A picture of the CNT film transferred on top of the Kapton substrate using the above technique is shown in Figure 24(d).

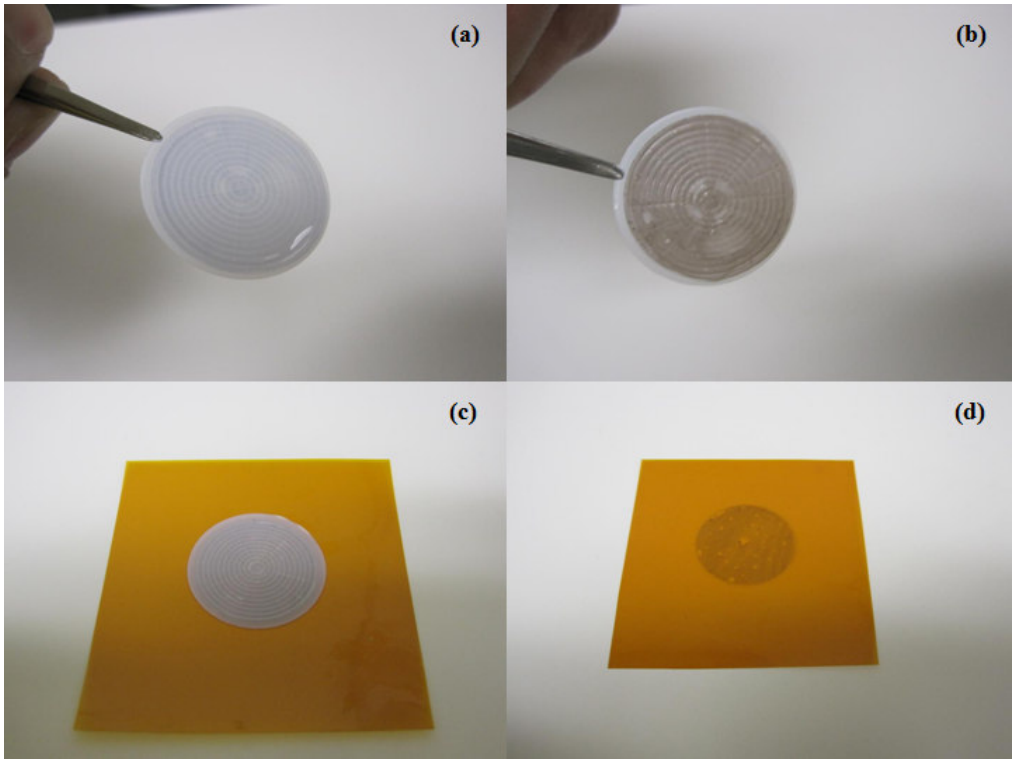

Figure 24: After passing CNT solution through the filter, (a) back-side picture, (b) Front-side picture, (c) Treated filter placed upside down on Kapton, (d) CNT film on Kapton after dissolving filter using acetone vapors.

For the above demonstration, a high concentration of CNT was used (as specified in statement (a) above) in order to clearly show the film. The film with a very low concentration of CNT in water forms a transparent thin film that is difficult to see with the naked eye.

Figure 25 shows the scanning electron microscope (SEM) image of the CNTs from Nanointegris on a glass substrate coated with Au:Pd (60:40). A glass substrate was used for SEM imaging since the high energy of the electron beam causes bending to the

Kapton substrate at high resolution. The image cannot be focused if using Kapton substrate.

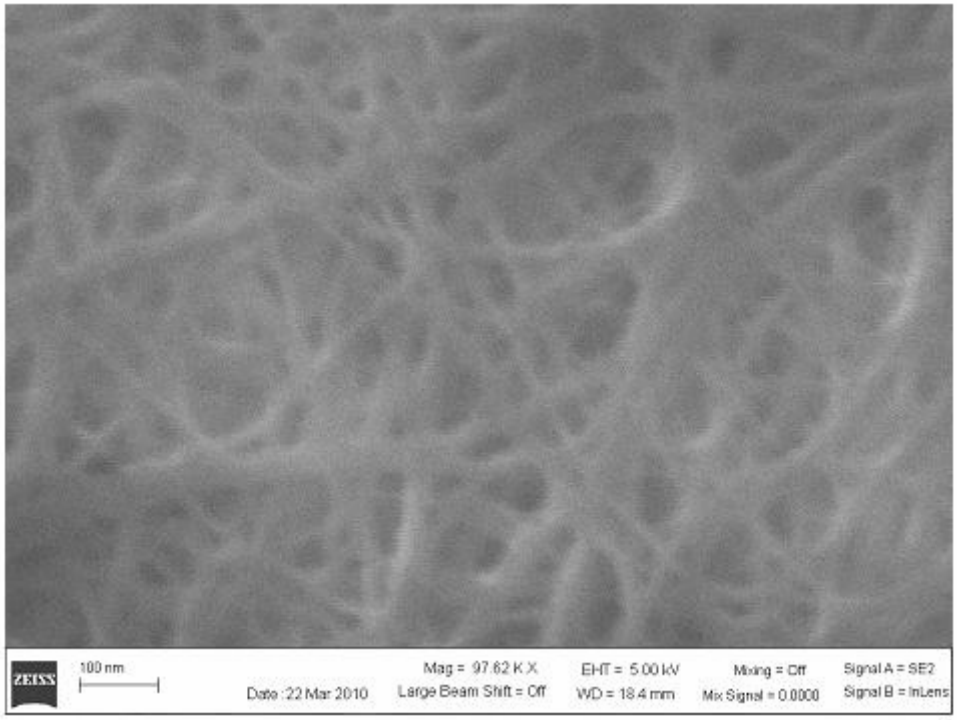

Figure 25: SEM image of CNT from Nanointegris on glass substrate.

2. Aligned CNT thin film

The CNT solution obtained from Nanointegris contains surfactant; the solution has a light purple color and is clear of particles. While all CNT solutions obtained from other vendors, particles can be seen through the glass bottles. The clear CNT solution from Nanointegris indicates the CNTs in the solution are not clustering together due to the presence of surfactants. Knowing that 2-propanol alcohol is used to "release" the surfactants from the CNTs, a droplet of the alcohol was applied to a diluted CNT solution

from Nanointegris. As soon as alcohol dissolves into the CNT solution, fine black particles appeared in the liquid.

Since the CNTs were separated from each other, a dip-coat technique was used to deposit the CNTs on the substrate. This technique yields multiple uniform layers of CNT thin film on the substrate. Figure 26 shows the schematic of the dip coating or the traditional Langmuir-Schaeffer [3]. This technique has been used widely in the past to deposit particles on a surface. Depending on the drying speed and particle concentration and size, a single layer or multiple layers of particles can be obtained.

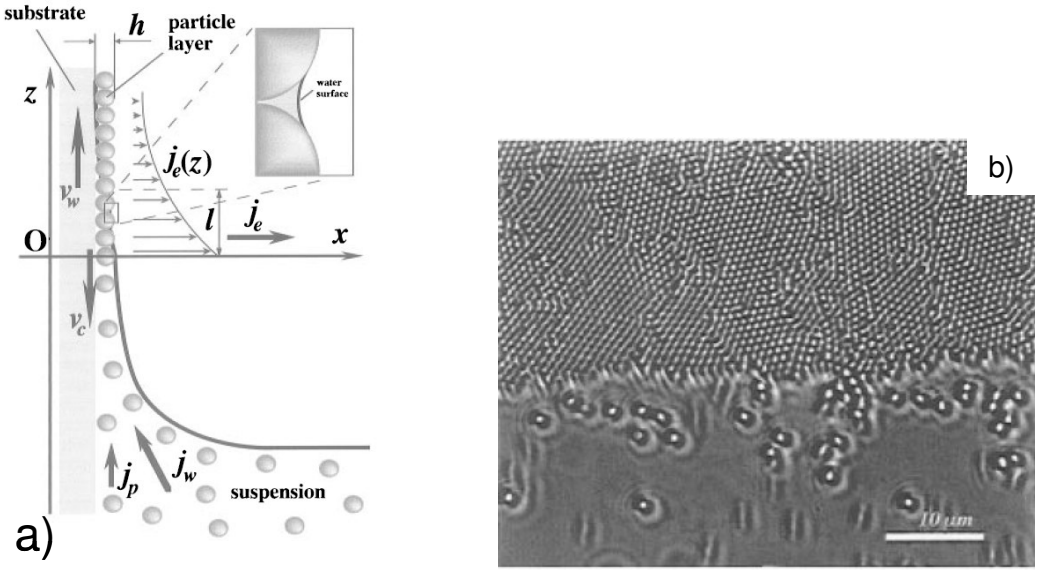

Figure 26: a) Schematic of the dip coating technique. Layers of particles grow on the substrate plate that is being withdrawn from a suspension. b) Particle monolayer grows on the substrate plate that is withdrawn from a suspension. The lower half of the picture shows particles dragged by the water flow toward the forming monolayer. Particles are seen as short fuzzy lines due to the high velocity in the microscale [4].

The main driving force for the convective transfer of particles is the evaporation of the solvent. When the solvent vapor pressure saturates (at equilibrium), the pressure balance in a small bulk volume inside the wetting film is given by [4]

$$\Pi + P_{CP} = P_C + P_h \tag{1}$$

where Π is the sum of the van der Waals and electrostatic disjoining pressure for the suspension wetting films on the substrate surface, P_{CP} is the capillary pressure due to the curvature of the liquid surface between neighboring particles in particle film, P_C is the reference capillary pressure, and $P_h = \Delta\rho g h_C$ is the hydrostatic pressure in a vertical film.

As the solvent starts to evaporate and the substrate is withdrawn from a suspension, the pressure gradient, ΔP, produces a suspension influx from the bulk suspension toward the wetting suspension film given by [4]

$$\Delta P = \left(\Pi + P_{CP}\right) - \left(P_C + P_h\right) \tag{2}$$

This influx consists of a solvent component, j_w, and a particle flux component, j_p. The solvent flux j_w compensates for the solvent evaporated from the film j_e and the particle flux j_p, causing the particles to accumulate in the film and form a dense structure. The accumulation rate of the particle, v_c, has been proposed by Dimitrov and Nagayama [3]

$$v_c = \frac{j_e l \phi}{h(1-\varepsilon)(1-\phi)} \tag{3}$$

where: ε and h are the porosity and height of the particle, ϕ is the volume fraction of the particles in suspension and j_e is the solvent evaporation rate. From the equation, the

monolayer growth rate of the particle depends on the particle volume fraction, ϕ; solvent evaporation rate, j_e; height of the particle h (in case of monolayer of particle h = diameter of the particle), porosity, ε; and the evaporation length l.

A CNT solution from NanoIntegris was deposited on a small piece of silicon wafer using the dip-coat technique as described above. The SEM images of the CNT thin film formation are shown in Figure 27. Stripes of CNT can be seen on the substrate due to the fast drying speed. A magnified SEM image of the aligned CNTs with the water contact line (or solid-vapor-liquid interface) is also shown. As the liquid evaporates, the convective force transfers the CNTs to the contact line, after which they deposit on the substrate. As the evaporation proceeds, the capillary force, which pulls the liquid inward, builds up and eventually breaks up when it is greater than the surface tension of the liquid. When the force breakup occurs, a new contact line is formed. This process happens at high drying speeds. The stripe thickness can be controlled by temperature, solvent properties, particle densities, and the substrate surface roughness.

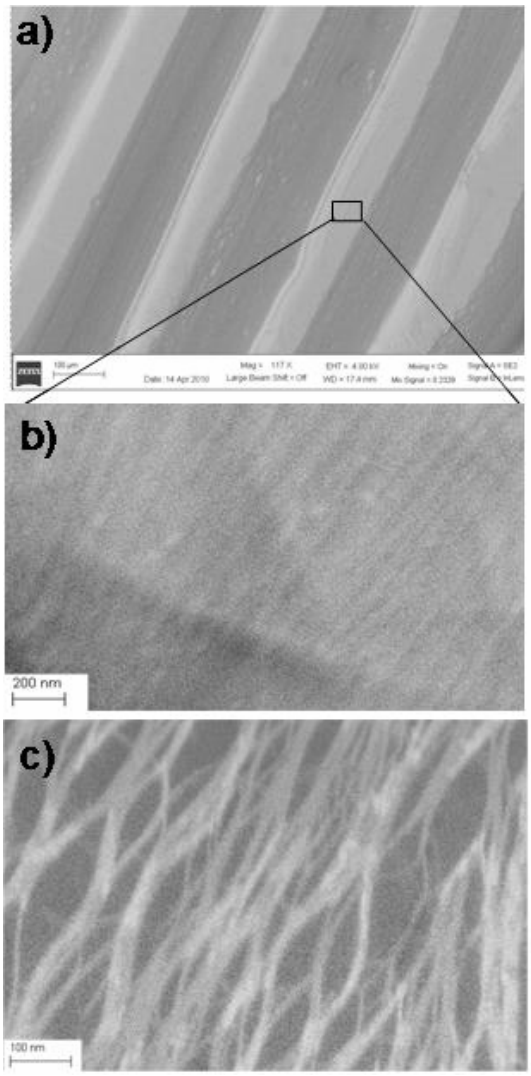

Figure 27: SEM image of self-aligned CNTs deposited on silicon surface using dip-coat technique.

As mentioned in the integration, special Kapton film with adhesive coating on one side is used to capture self-aligned CNT film. This capture CNT film is transferred onto the device channel region on the Kapton subtrate. CNT stripes (width in hundred of microns) formed during the dip coat technique might cause non-uniformity on CNT density. A modified dip coat technique has been developed to provide a uniform CNT

film in large area rather than stripes. Similar self-aligned CNT is observed when using multiple small pieces of silicon wafers placed next to each others in a small gap. Figure 28 shows the schematic cross section of the technique utilizing the capillary effect. The liquid rises in between narrow gap. Using this technique, aligned CNT film can be formed without using a large volume of CNT solution.

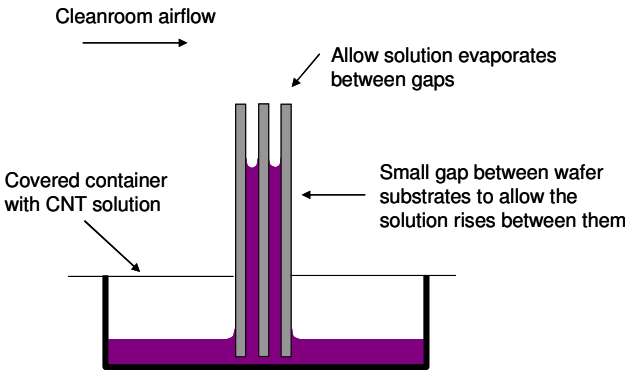

Figure 28: Schematic cross section of modified dip coat technique. The capillary pressure causes the CNT solution rises between wafer substrate covering a large area of the wafers using minimum volume of CNT solution.

Figure 29 shows series of pictures describe the modifying dip coat technique to form self-aligned CNT on large area using a minimum volume of CNT solution. From Figure 29.c, CNT solution rises between plates due to the capillary pressure. As the evaporation of the CNT solution occurs between gaps, the CNT is transported into the water contact line (between the wafers' gap). Using this technique, multiple wafer pieces can be deposited with self-aligned CNT film in large area using less CNT solution. The technique is described in detail below:

- Small pieces of thick Kapton tape (2x 125μm) are glued on the wafer pieces to separate them from each other. For demonstration the first piece is glass substrate (Figure 29.a).
- These wafer pieces are taped together by thin Kapton tape (Figure 29.b)
- Then, they are placed on the glass container with small amount of CNT solution. Due to capillary pressure, the liquid rises quickly between the wafer pieces. The glass container is sealed with glass plates and tape allowing liquid to evaporate only between wafer's gaps. The set up is placed under cleanroom vent hood and the CNT solution is allowed to dry (Figure 29.c). After drying, a large CNT thin film is observed on the wafer substrate as shown in the inlet picture, as shown in Figure 29.c.

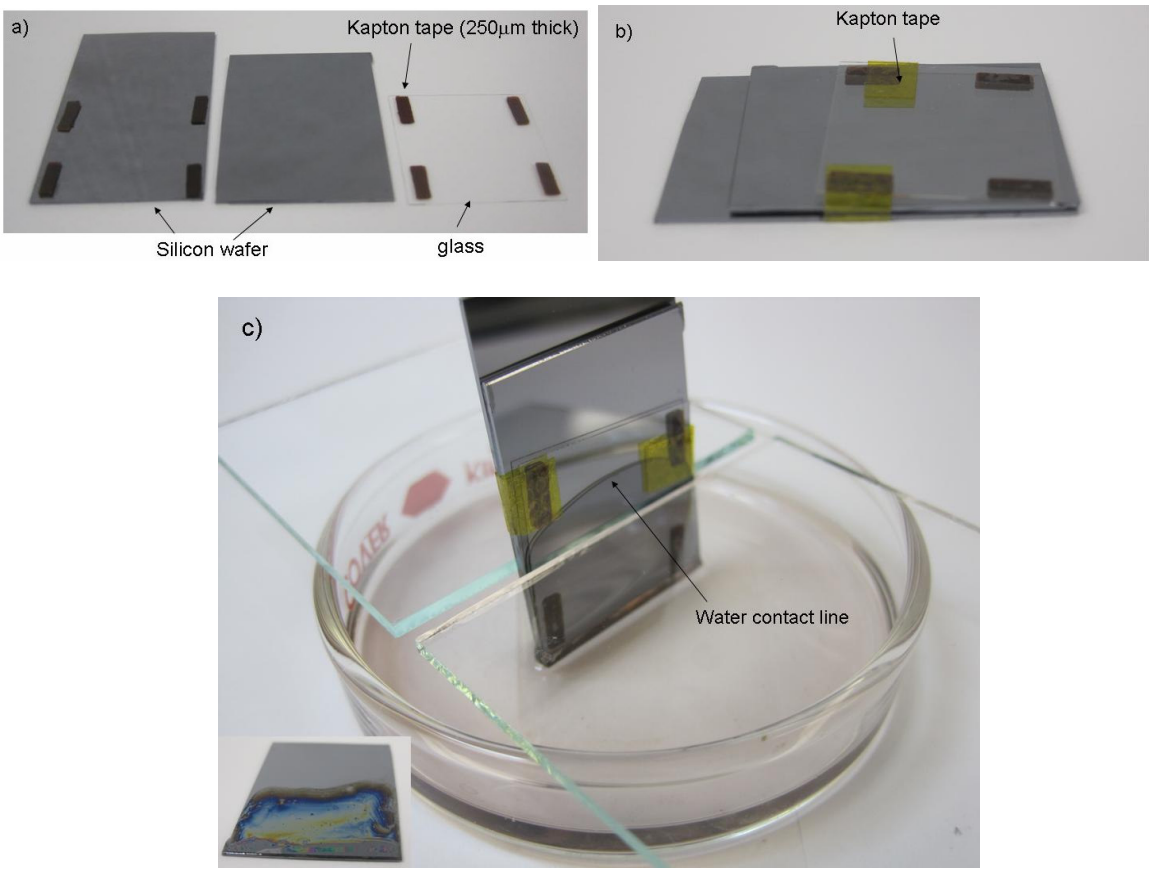

Figure 29: : a) Thick Kapton tapes are glued on wafers to keep wafer separate from each others, b) wafer pieces are taped together to make gap between them, c) liquid solution rises between glass and wafer piece. Inlet picture shows wafer piece after solution dry.

Figure 30 shows SEM image of self-aligned CNT by using modified technique. Notice that the CNTs are not aligned in parallel with the liquid contact line but rather somewhat perpendicular to the liquid contact line. The narrow gap between to two wafers and slow evaporation rate of the solvent might cause different aligning orientation. Notice that the surfactant prevents the CNT from bundling with each other.

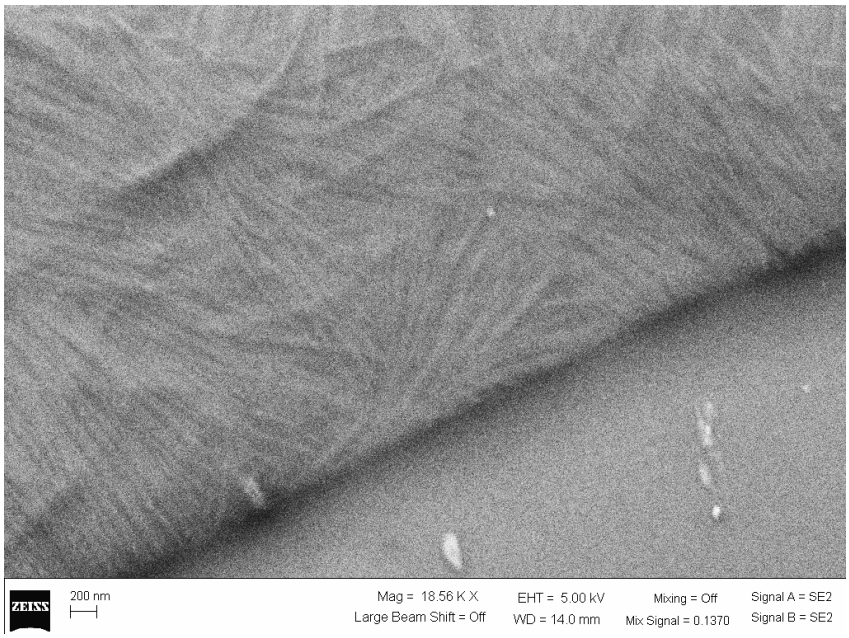

Figure 30: Aligned CNT using modified dip coat technique.

In summary, random and self-aligned CNT thin films have been fabricated for CNT TFT device fabrication. Modified dip coat technique provides similar result of self-aligned CNTs but using less CNT solution.

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Chapter 4: Fabrication Process

I. Introduction

Ink-jet printing is a non-contact printing technology in which droplets of ink are jetted from a small aperture directly to a specified position on a media to create an image. It is a simple, cost effective method to produce electronics and an attractive process for flexible electronics due to its non-contact and additive deposition technique. The technique does not require sacrificial resist or liftoff layers, but rather deposits materials only when needed.

The ink-jet printer used in this research is a Fujifilm Dimatix Materials Printer (DMP-2800), as shown in Figure. 31 This printer uses piezoelectric printing cartridge (DMC-11610). The ink droplet dispensed from the ink cartridge has a nominal volume of 10pL. The machine is suitable to print circuits on a variety of substrates, including flexible substrates, since the printing is performed at room temperature. Additionally, since it is a non-contact printing technique, the substrate topography is not an issue for the deposition. This printing technique, therefore, can also fill the contact "via" during multi-layer interconnection without any problems or print multiple layers of different materials on top of each others.

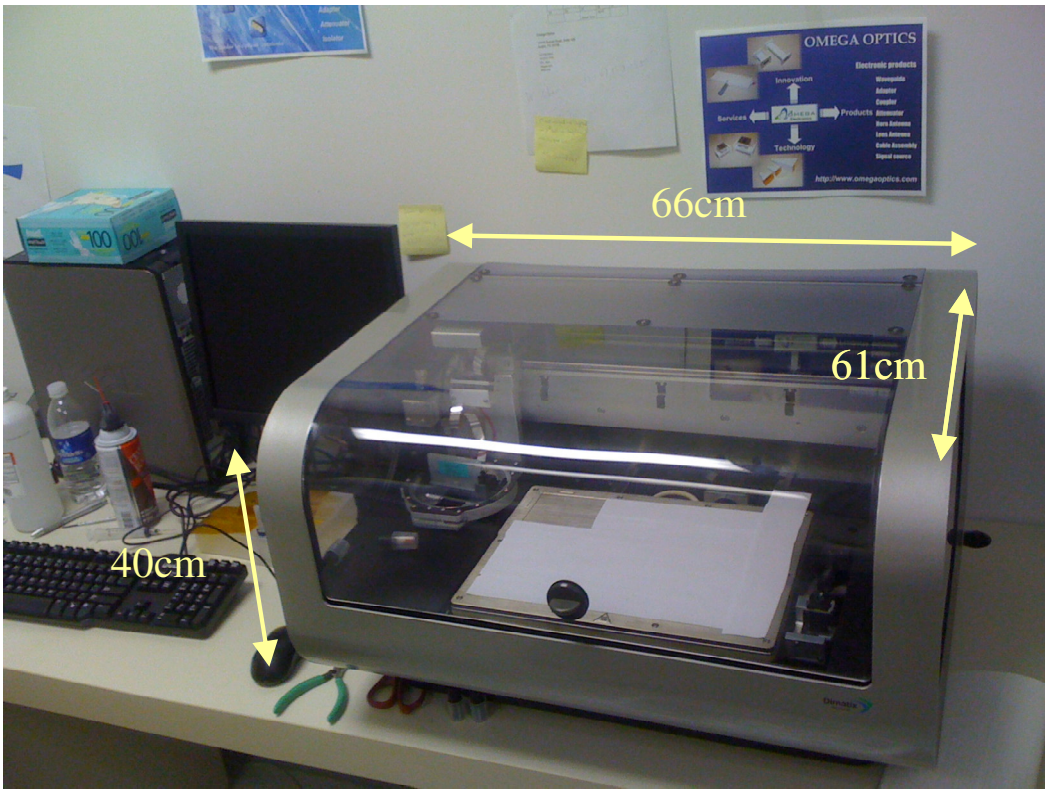


Figure 31: Fujifilm Dimatix Materials Printer (DMP-2800).

The printing head consists of 16 nozzles that can jet ink out simultaneously. The diameter of each nozzle is approximately 21µm. The ink-jet operates based on piezo MEMS ink jet technology. It is possible to tilt the angle of the printing head with respect to the plane of the substrate in order to control the resolution of the image. Figure 32 shows the effect of cartridge angle on the printing resolution. Smaller cartridge angle will provide high printing resolution (ink density or thicker material deposit). The cartridge angle is calculated and provided by internal software controlling the printer when the image printing file is loaded, and printing resolution value is entered.

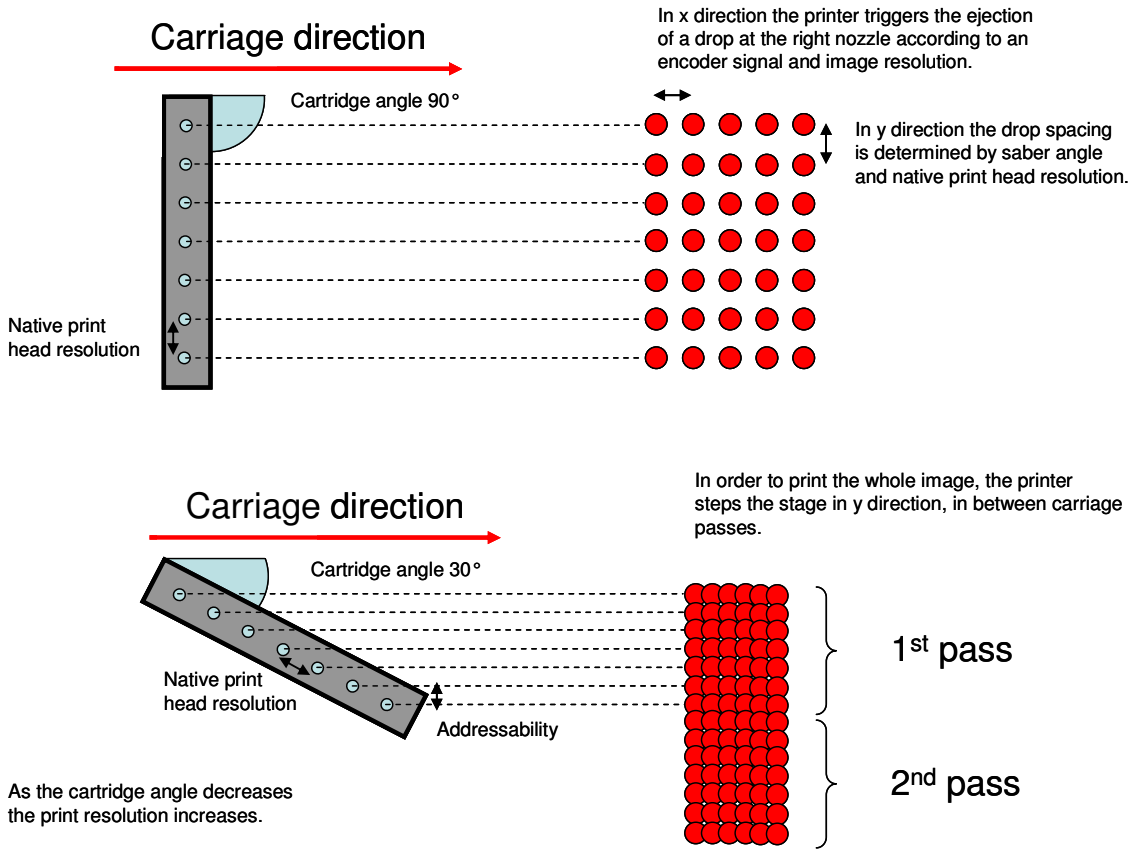


Figure 32: Schematic of cartridge angle versus printing resolution. Smaller cartridge angle can provide higher printing resolution.

Figure 33 shows the schematic of the piezo MEMS ink jet technology operation. A predetermined voltage waveform is applied in three phases to each of the 16 piezo electric MEMS valves controlling the nozzles in order to form a droplet. Figure 33.a shows the start or standby position of the pumping chamber before the jet pulse begins. The fluid chamber is depressed by the bias voltage. In Phase I, at the beginning of each jetting cycle, the decrease in voltage to zero volts brings the piezo MEM back to a neutral, straight and relaxed position at its maximum volume (Figure 33.b). The next two phases, Phase 2 and Phase 3, of the cycle are the drop ejection phase. The chamber is

compressed and pressure generated to eject a drop (Figure 33.c). The PZT motion is controlled in order to form a droplet, but due to the surface tension of the fluid, does not detach from the cartridge. Phase 4 is the recovery phase where the piezo voltage is brought back down to its bias level. The chamber decompresses, which causes the pull back of the ejected drop at the nozzle. The droplet is separated from the nozzle and deposited on the substrate (Figure 33.d) [1].

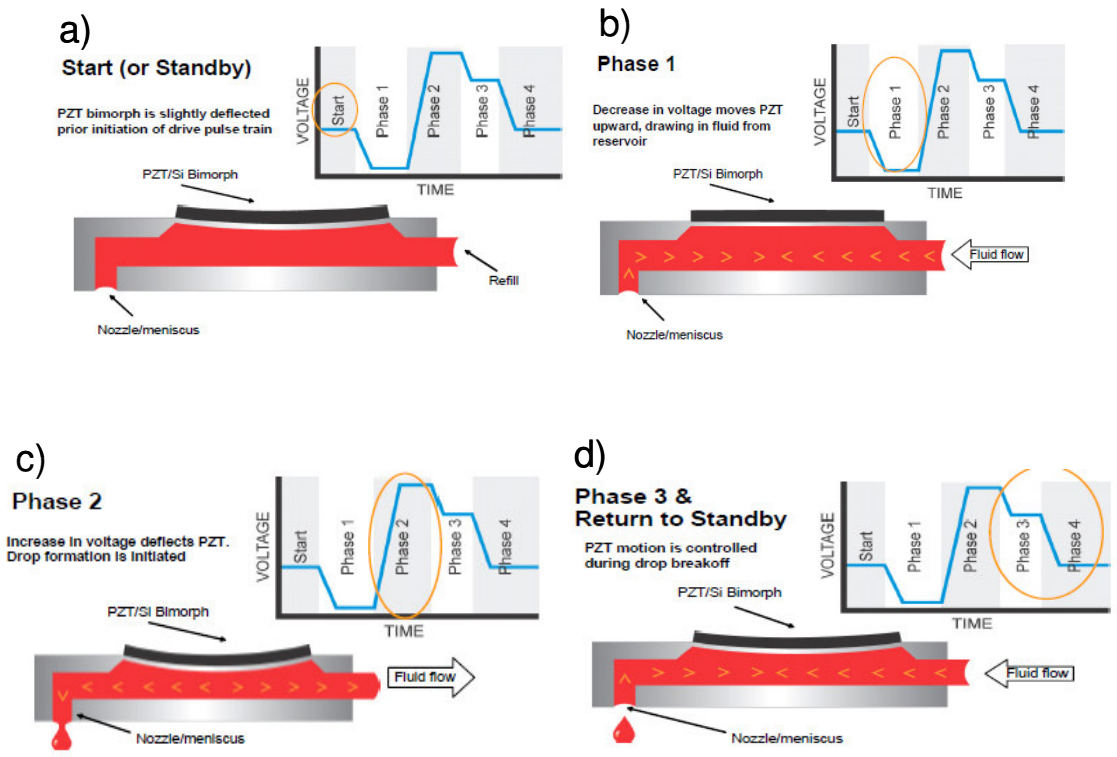


Figure 33: Formation of a droplet in the nozzle [1] .

Understanding the operation of the cartridge helped in designing the waveform for each type of material ink during this research. Notice that the drop is formed (in Figure 33.c) at the tip of the nozzle. As will be discussed below, for long operation time

or when printing small lines or structure next to large structure, the ink can be jetted irregularly due to the tip of the nozzle getting wet by liquid ink.

II. Device fabrication by ink-jet printing

3. Flexible electronics fabrication by printing process

Topics discussed in this section are outside of the printer's manual, serving as a guide for flexible electronics fabrication by ink-jet printing technique. Printing seems to be an easy task; however, to print a large circuit device, it is not easy as thought. As mentioned earlier, the cartridge has 16 nozzles. However, in order to prevent deviation in the operation of these nozzles, testing of each nozzle is needed before any printing job. It was found out that for small line or structure, usage of one nozzle provides more consistent results than using multiple nozzles. Several other reports are also consistent with this finding [2,3].

For large area printing, with small and large structures or lines next to each other, the orientation of the device or circuit needs to be considered such that the printing material can be deposited uniformly. It is found that printing small line and large area that are located next to each other together produces a poor device. This is because, during large area printing, the nozzles operate continuously, and the printing material wets the nozzle surface (due to long jetting time). Thus, when printing on small area or small line, the wet liquid ink on nozzle surface causes the jet to be misfired. Additionally, it was also found that at start, the nozzle provides uniform deposition. After printing a large area, the

performance degrades. Figure 34 below shows the landscape and portrait orientations of the Phased-Array Antenna (PAA) system. The transmission lines of each antenna elements need to have the same resistance for uniform power delivery to the antenna elements. Using landscape orientation, the ink-jet starts printing the PAA system from the RF input element, and then branches out to each antenna elements. Therefore, the ink is distributed evenly into each antenna branches. On the contrary, if a portrait orientation is used, the transmission lines are printed together with large antenna elements. This causes the first and last transmission lines to have different resistances due to the cartridge performance degradation after printing large area.

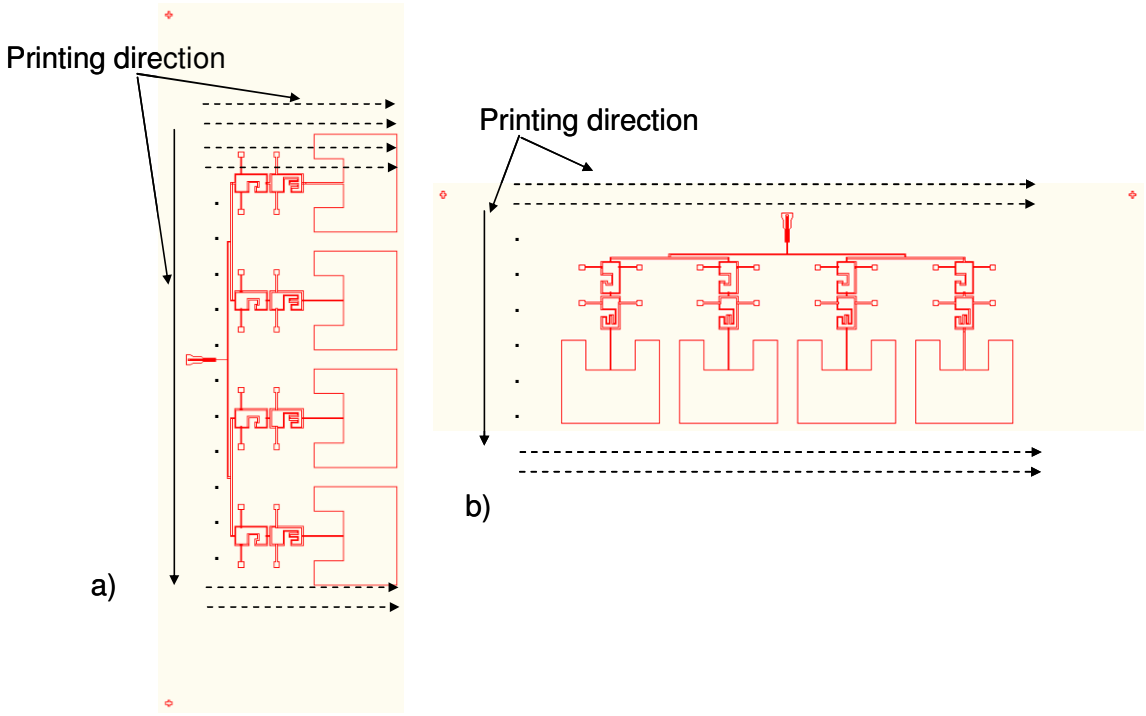


Figure 34: (a) Portrait and (b) landscape orientation of phased-array antenna system. Per printing direction, landscape orientation provides better uniformity material deposition between transmission lines.

Breaking down the printing area to several small parts is also a good way to have better uniform printing. Figure 35 shows PAA system broken down into 2 parts, as indicated by the blue and red regions. The first part (red area) contains narrow width (~300micron) transmission lines. This part can be printed by using a single nozzle on the cartridge for better precision. The second part (blue area) consists of the large antenna elements, which can be printed using multiple nozzles. Using this type of combination printing, the printed product has better precision and is performed with an optimal printing time. Please note that alignment marks are used to precisely align the two printing steps, which are also shown in the Figure 35 as crosses on the top left and right corners.

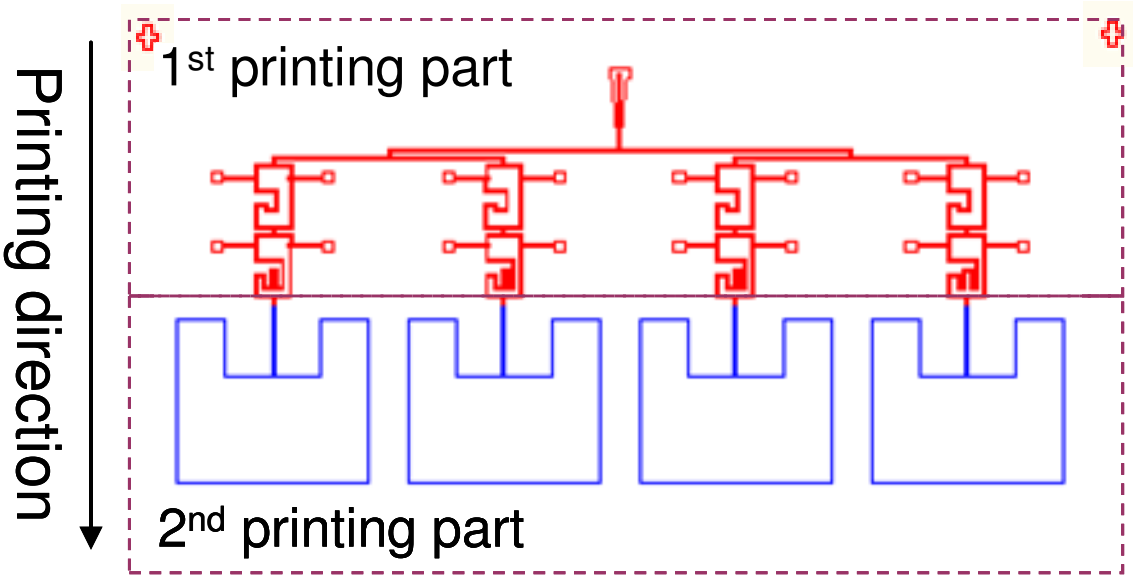


Figure 35: Schematic of a 2-bit, 1x4 Phased-Array Antenna. Printing transmission lines and antenna elements separately provides good printing coverage.

4. Resolution limit

The minimum line width and spacing dimensions specified by manufacturer are 100µm using their specified model ink. However, for "wet" ink which can spread quickly on the substrate, the line can be bigger than specified.

Silver ink from Cabot Corporation (CCI-300) is used through out the research (see material evaluation below) for transmission lines, antenna elements, interconnects etc. Using this silver ink, the minimum line width achievable is around 65µm, as shown in Figure 36. This minimum line width is due to the slightly higher viscosity of silver ink compared to the model ink. The single silver droplet on the substrate yields a diameter of ~47µm after annealing. To achieve these minimum structure sizes, minimum separation between cartridge nozzles and substrate, and minimum waveform voltage of 26V are used.

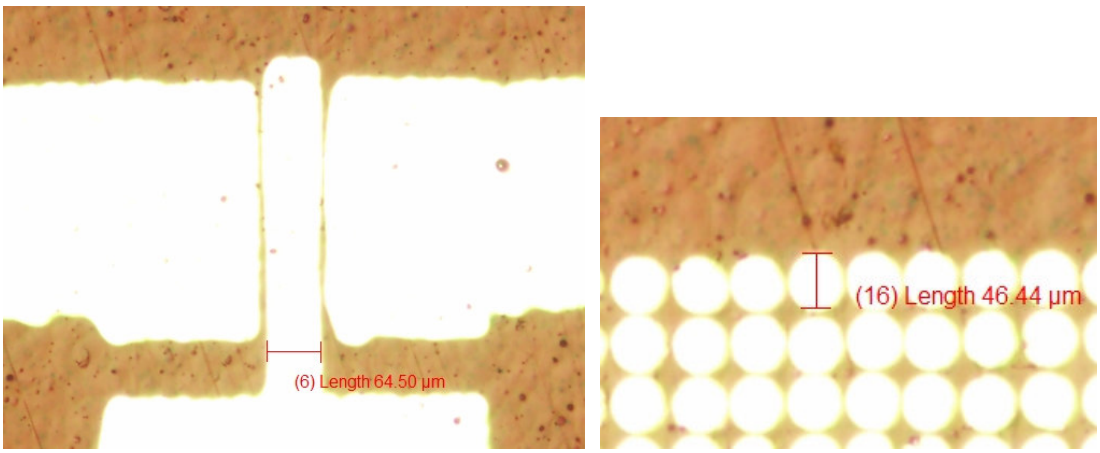


Figure 36: Minimum line width of 65µm can be achieved using Dimatix printer. The silver ink used in this study yields a droplet size of 47µm after annealing.

5. Material evaluation

Below are the evaluation results for the electrodes, dielectric layer and active layers for the CNT TFT

a. Silver Ink Evaluation:

For the source, drain and gate electrodes, silver ink from two vendors, E-ink and Cabot Corporation, were evaluated. In order to determine the performance of the silver ink, metal patterns were printed, as shown in Figure. 37. Evaluation of these metal patterns is important because these form electrodes, electrical interconnects, transmission lines, resistors and antenna elements.

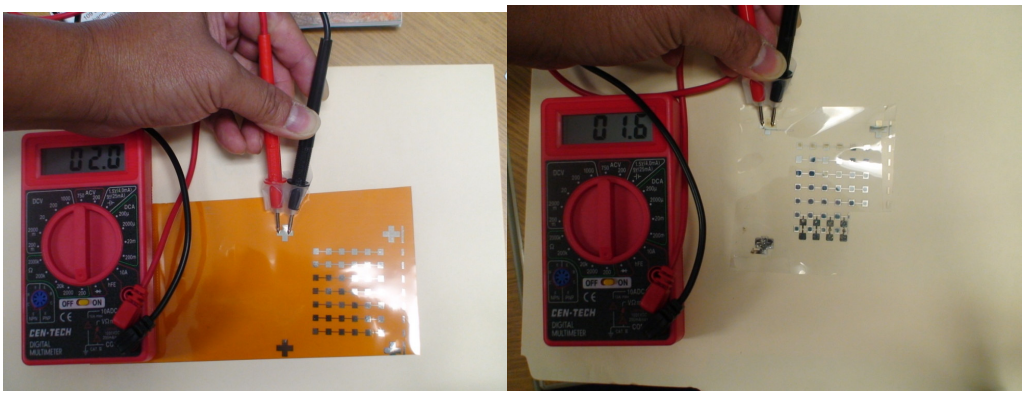


Figure 37: Patterns printed using (a) E-ink from Fujifilm and (b) Cabot Corporation.

The resistances of the two metal patterns were measured to be 1.6 Ohm and 2.0 Ohm for E-ink and Cabot ink, respectively. The two patterns were annealed at 150^0C and the resistance was measured as a function of annealing time. The measured resistance of Cabot ink as a function of annealing time is shown in Figure. 38. It can be seen that a lowest value of 1.1 Ohm was achieved after annealing for 4 minutes. Similarly, the lowest resistance achieved for E-ink was 1 Ohm after 3 minutes of annealing. Therefore,

after printing metal patterns in the circuit, these metal layers are annealed in order to achieve very low resistance. Due to commercial availability of Cabot ink, this ink is chosen for the entire architecture hereafter.

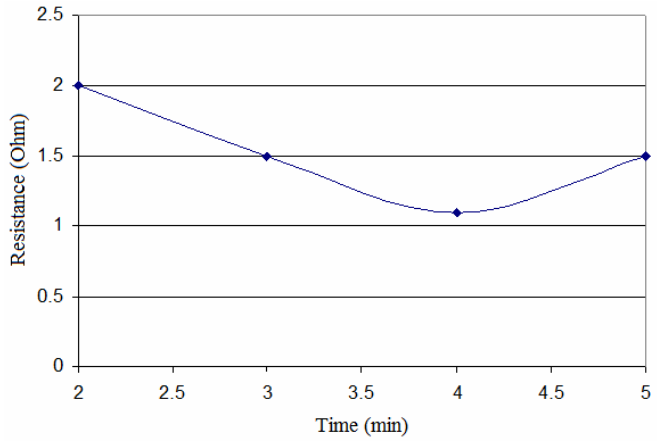


Figure 38: Measured resistance of Cabot ink as a function of annealing time at a temperature of 150^{0}C.

b. Dielectric Ink Evaluation:

Four different materials were considered for dielectric ink evaluation – 1) Spin-on glass, 2) Photoresist AZ5214, 3) SunChemical and Cellulose Acetate Butyrate (CAB) by Eastman.

First, Spin-on glass was tried as a dielectric. Spin-on glass showed very good adherence and easy to dry. However, the nozzles can be easy clogged when exposed to air. It is found that by properly storing the cartridge in a controlled environment, the material does not dry and clog up the nozzle; therefore, it can be reused in subsequence printing. Figure 39 shows the picture of spin-on glass fluid jetting out from the nozzles. The droplet spreads to 150µm diameter size on Kapton substrate.

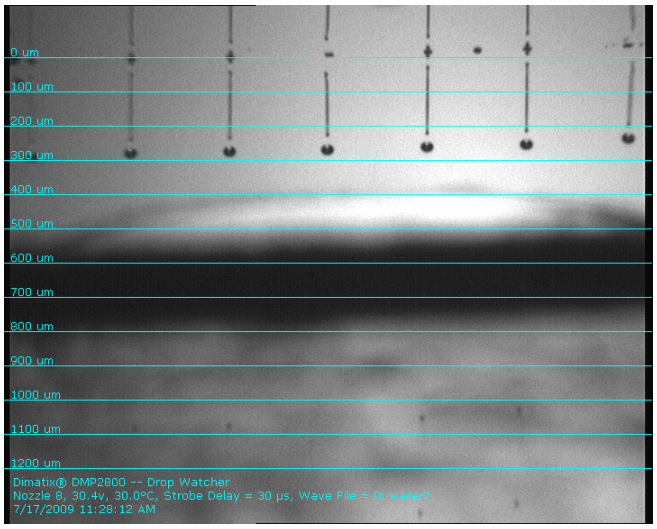


Figure 39: Good spin-on glass droplet jetted out of the cartridge's nozzles.

Photoresist AZ5214 was tried next as the dielectric material. The photoresist also showed excellent adherence to the first and subsequent layers. The photoresist did not clog up the nozzles even after prolonged use and also enabled reuse of the cartridge. Photo resist droplets from the cartridge are similar to spin-on glass. The diameter of the droplet is around 250µm indicating that its viscosity is smaller than spin-on glass material.

The dielectric ink from SunChemical required UV curing. A UV lamp from American UltraViolet was used for the experiments. The UV system has a maximum output power of 100W. When the output from the UV source was used to cure the dielectric from a very small working distance, it was found that the excess power caused heating and burning effects on the substrate, as shown in Figure 40. Since the power on the machine was fixed, two other parameters were controlled in order to give a good cure – 1) operating distance and 2) exposure time.

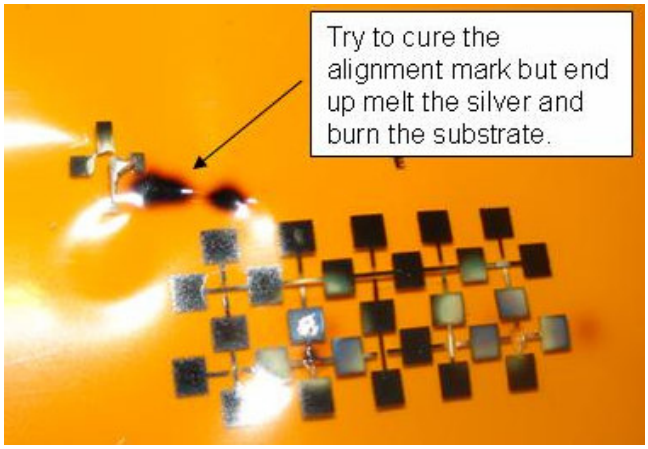


Figure 40: Effect of high power UV on the flexible substrate.

From several trials, a working distance of around 4in -6in from the UV light source to the substrate was found to give good results, as shown in Figure 41.

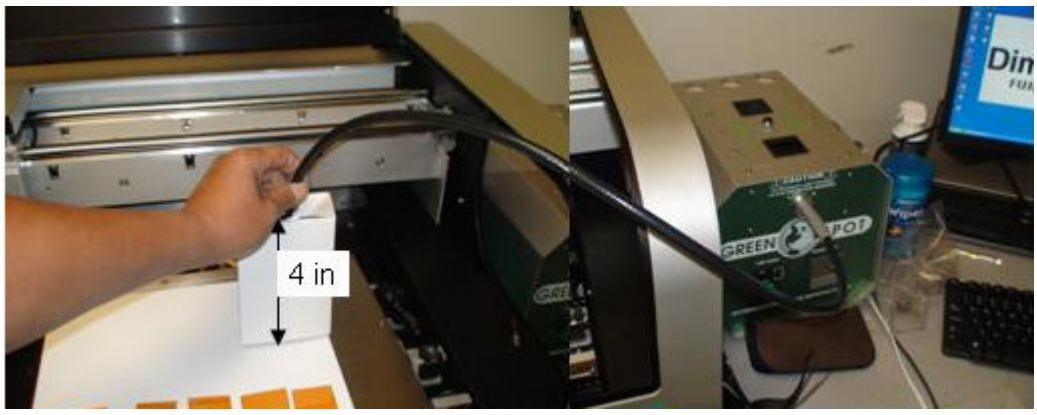


Figure 41: Working distance of 4"-6" gives good results.

For the exposure time control, different exposure times and number of shots were controlled in order to cure the dielectric with minimal or no deformation of the substrate. Table 2 summarizes the results of exposure conditions on the cure. For single shot, exposure times of 5s, 10s, and 15s do not sufficiently dry the solvent in the dielectric. Further time to about 20s cures the dielectric, but the substrate deforms due to excess heat

from the UV source. Figure 42(a) shows the effect of a 20s single shot exposure on the curing result. Although the dielectric is cured, the substrate is deformed

Single cure		**Multiple at 5s each**	
5s	Wet	1x5s	Wet
10s	Wet	2x5s	Wet
15s	Wet	3x5s	Wet
20s	Dry (substrate deforms more)	4x5s	Dry (no substrate deformation)

Table 2: Effect of exposure conditions on dielectric curing.

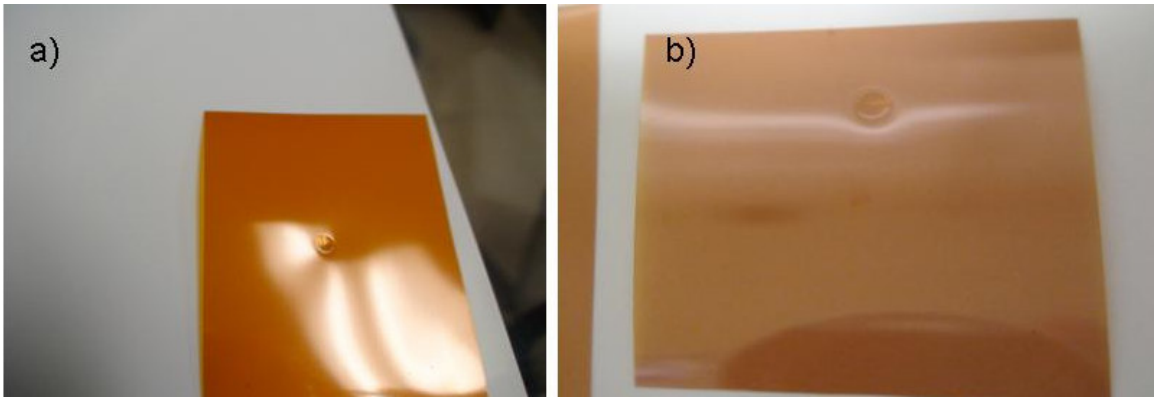


Figure 42: (a) 20s single shot exposure deforms the substrate (b) 4 shots of 5s each does not deform the substrate.

When multiple shots of 5s durations are used, no deformation of the substrate is observed. For the UV curable dielectric, 4 shots of 5s duration yields a very good result, as shown in Figure 42(b).

The last dielectric material, Cellulose Acetate Butyrate (CAB) by Eastman, was also evaluated. This material can be dissolved into acetone and a multitude of other

solvents. The deposited film using CAB in Acetone dries up quickly, and subsequent layers can be easily deposited on it (similar surface potential as the Kapton surface) in order to achieve any thickness of the dielectric.

Table 3 shows the summary of the dielectric ink evaluation. Photo resist and spin-on glass material are chosen as the dielectric materials for this work due to their good compatibility with the printing cartridge.

Dielectric Ink	**Advantage**	**Disadvantage**
Photoresist (AZ5214)	Printable, good coverage, thermal curing, silver ink can be printed on	
Spin-on-glass	Printable, good coverage, low gate leakage (pA)	Clog nozzle when dry
SunChemical	Printable, good coverage, low gate leakage (pA)	UV cure, hydrophobic surface, deform the substrate if over curing
Cellulose Acetate Butyrate (CAB)	Low leakage, hydrophilic surface (uniform particle deposition surface)	Acetone or benzene solvents.

Table 3: Summary of dielectric evaluation

c. Carbon Nanotube (CNT) Ink Evaluation:

Three different CNT solutions are obtained for the evaluation, from Brewer Science, Cheap Tubes and NanoIntegris, Inc.

CNT solution from Brewer Science is a 99% pure, SWCNT 0.7μm length, 2:1 ratio semiconducting / metallic tubes dispersed in water. In a new printing cartridge, CNT solution can be jetted out, but it is often clogs the cartridge. However, due to low concentration of CNT in the ink, many layers of CNT need to be printed in order to observe appreciable current in the FET device. Before filling the CNT solution into the printing cartridge, the CNT solution container is placed into the megasonic cleaning tub for 30 minutes. The solution is then filled into the cartridge without filtering due to the size of the CNT (filter is used for other solutions during cartridge filling). Figure 43 below shows the camera pictures of CNT droplet jetted out from printer cartridge at different stages.

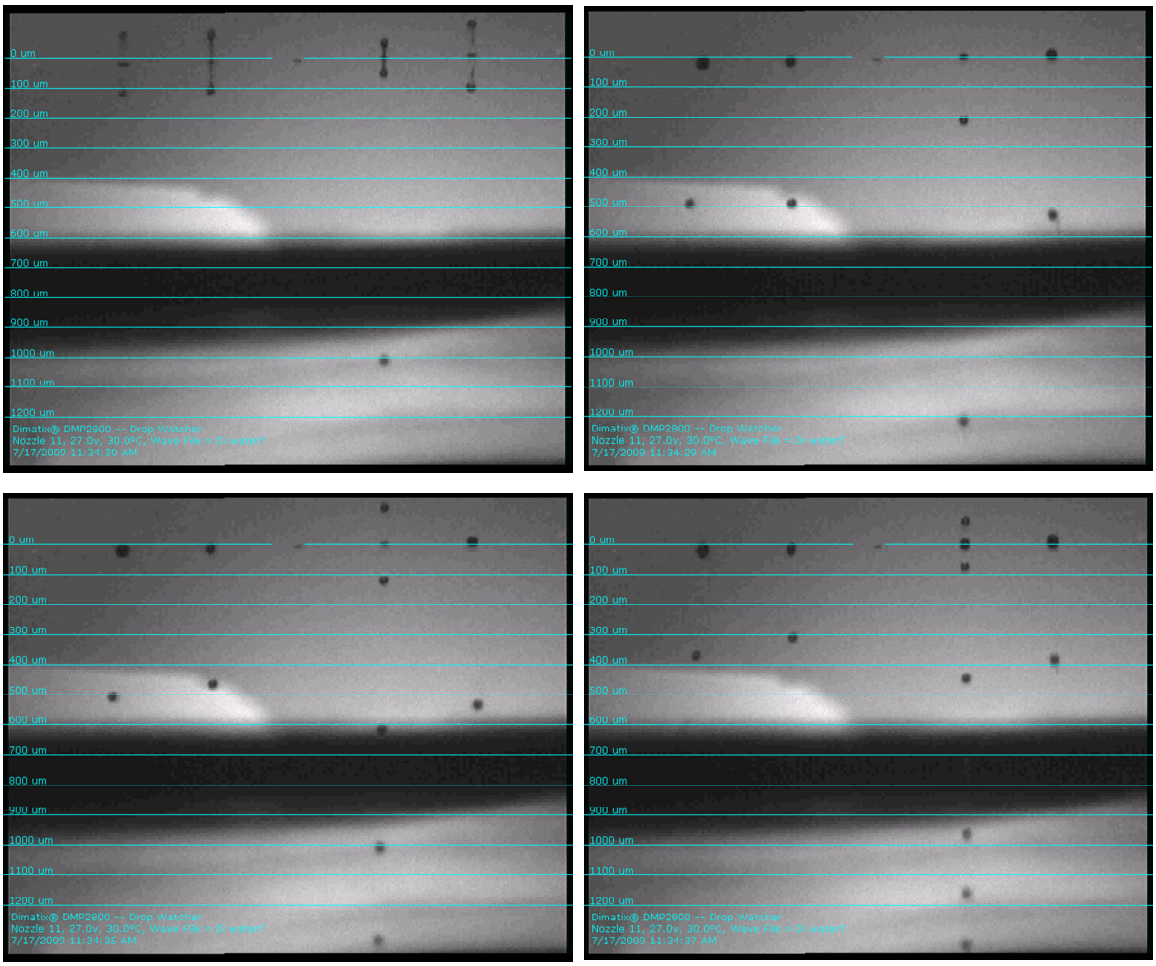


Figure 43: Camera pictures of CNT droplet from Brewer Science jetted out of cartridge's nozzles. Non-uniform jetting is observed.

From the above Figure 43, CNT droplets are jetted out from 4 nozzles non-uniformly despite the effort of changing waveform voltage and jetting frequency. This indicates that the CNT solution is very hard to print using ink-jet printing technique especially from DMC-11610 cartridge for Dimatix printer. The cartridge is clogged very often. High pressure air is used to unclog the nozzles as shown in Figure 44; however, this is not a permanent solution.

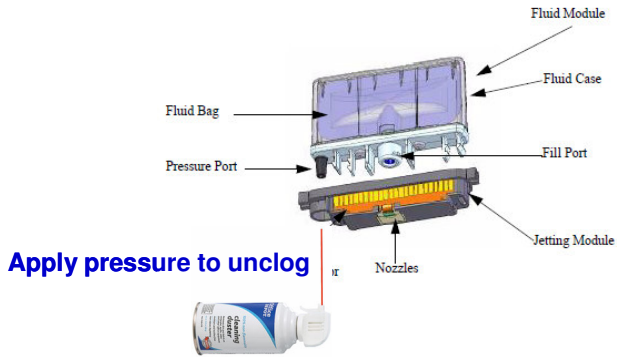


Figure 44: Un-clog the cartridge nozzles by high air pressure.

CNT solutions from Cheap Tubes, Inc. were also obtained. These CNT solutions contain CNTs with functionalized group molecules. Depending on the type of functional group added, the CNT can behave as a P-type or an N-type semiconductor. Table 4 shows a list of functional groups that can be added to either remove an electron or donate an electron.

Electron-withdrawing function groups	Electron-donating function groups
-COOR, -COOH, -COR, -CHO, $-NO_2$, -CN -F, -Cl, -BR, -I, $-CF_3$ (where, R represents the group $-CH_3$)	-OH, $-NH_2$, $-NR_2$, -SH, $-CR_3$, -OR (where, R represents the group $-CH_3$)

Table 4: Electron-withdrawing and Electron-donating functional groups.

CNT solution from NanoIntegris is a 99% pure semiconducting single walled carbon nanotubes in surfactant solvent (S10-671, 0.1mg in 10mL aqueous solution). The solution has a light purple color and is clear of particles. With all CNT solutions obtained from other vendors, particles can be seen through the glass bottles. The clear CNT

solution from Nanointegris indicates that the CNTs in the solution are not clustering together due to the presence of surfactants. Knowing that 2-propanol alcohol is used to "release" the surfactants from the CNTs, a droplet of the alcohol was applied to a diluted CNT solution from Nanointegris. As soon as the alcohol dissolved into the CNT solution, fine black particles appeared in the liquid.

Similar to CNT solution from Brewer Science, the CNT solution from NanoIntegris can also be used as an ink. Clogging problem is still observed on this solution. However, the CNT solution contains surfactant. After printing this solution, alcohol is needed to apply on the film to remove the surfactant. As discussed in chapter 2, this solution has been used to form self-aligned CNT thin film.

Table 5 shows the summary of the CNT solution evaluation. From chapter 2, CNT solutions from Brewer Science and NanoIntergris provide working results.

CNT solution	Advantage	Disadvantage
Brewer Science	98% pure semiconducting CNT in water solution, printable	CNT clustering, clog ink-jet nozzle
NanoIntegris	99% pure semiconducting CNT in surfactant solution, printable. **In high concentration of surfactant solution ⇒ keep CNTs separate**	High concentration of surfactants
Cheap Tube	CNT solution with different functionality groups	High concentration in water solution, visible particles

Table 5: Summary CNT solution evaluation

d. Kapton Substrate

Kapton film (HN type) from Dupont is used as substrate of the research. This Kapton film can be used at temperatures as low as -269^{o}C and as high as 400^{o}C per its specification. Three different film thicknesses are evaluated 50μm, 75μm, and 125μm. A 25 micron and 125 micron thick Kapton films with adhesive coating on one side are also obtained for the multilayer integration development. Kapton film is chosen as the substrate for this work due to its high temperature operability and low elastic coefficient of the material. Since it is less stretchable, the bending tests on CNT-TFT or via show less variation in performance.

Reference

1. Fujifilm Dimatix Materials Printer (DMP-2800) operation manual

2. A. Rida, L. Yang, R. Vyas, M. Tentzeris, "Conductive Inkjet-Printed Antennas on Flexible Low-Cost Paper-based Substrates for RFID and WSN Apllications", IEEE Antennas and Propagation Magazine, Vol. 51, No. 3, 2009.

3. M. Tentzeris, R. Vyas, V. Lakafosis, A. Traille, A. Rida, G. Shaker, « Inkjet-Printed System-on-paper/polymer « Green » RFID and Wireless Sensors," Electronic Components and Technology Conferfence 2010, Proceeding 60th, pg. 1552-1555.

Chapter 5: Multilayer Metal Interconnect

I. Introduction

In order to develop full systems such as large area printed phased array antennas utilizing CNT-TFTs as RF amplifiers or switching elements, the signal layout scheme will be extremely complicated and prohibitive if performed in one dimension (i.e. all interconnection lines, other components and CNT-TFTs printed in the same layer). Similar to silicon semiconductor devices, such complex flexible electronics also require multiple layer metal interconnection strategy for its circuits. Especially, CNT-TFTs will all be formed in one layer and the signals will be routed to and from these FET to all other components through various stacked layers. In this chapter, the development and characterization of multilayer metal interconnection scheme will be presented. This technique utilizes the inkjet printing technique to fill metal ink inside interconnect via in order to connect metal lines on two different layers.

II. Integration

After forming the CNT-TFT device layer on the first substrate, a second special Kapton substrate (25μm thick), with an adhesive coated on one side, is bonded on top of the first substrate. Contact vias are formed on the second substrate prior to attaching, in order to enable metal filling and form metal contacts with the gate contact pads on the bottom substrate. The via diameter used in the work is 1mm (limited by the availability of cutting tool to cut the via with that size). The adhesion of this top substrate to the bottom substrate is critical since any voids between these layers will cause the liquid silver ink to

spread between these layers due to the capillary effects. Upon bonding these two layers together, an annealing process at 100°C for 30 minutes is performed under external pressure. Then, the silver metal interconnection lines are printed on the top Kapton layer. The printed silver ink penetrates through the vias to contact the gate contact pads on the bottom layer. Following this, another annealing process is performed in order to evaporate the solvent in the silver ink and form a good Ohmic contact. Figure 45 shows the schematic of multi-layer metal interconnect integration for flexible electronics performed in this work.

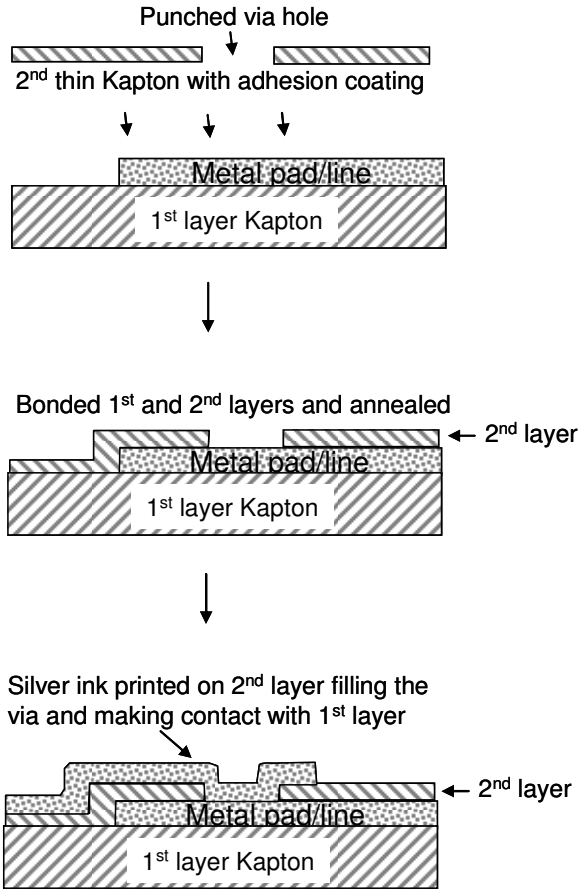


Figure 45: Multi-layer metal interconnect integration scheme.

Figures 46a and 46b show via development test structure, pre- and post silver ink printing on second Kapton layer. To protect the metal contact line and via, another Kapton substrate with adhesive coating is bonded on top (Figure 46c). This layer acts as a passivation or protection layer for the circuit and protects it from environment as well as provides good mechanical strength.

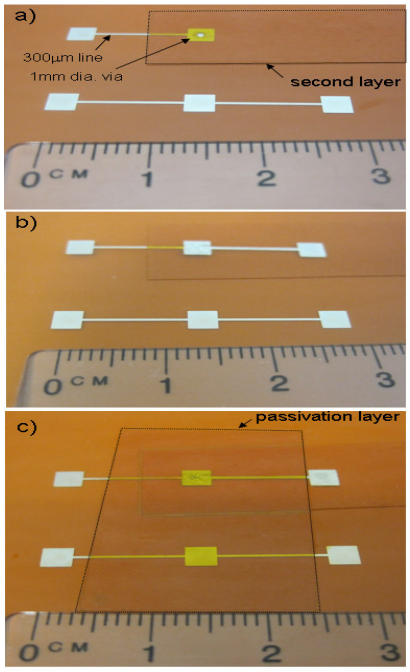


Figure 46: a) Via development test structure before forming via and second layer, b) Via formed and contact line was printed on second layer, c) Protected or passivation layer to protect the circuit.

III. Bending test

Figure 47 shows the bending test for via test structure using a similar set up shown in Chapter 2 for CNT-TFT's bending test (Figure 21). A lower resistance value is observed when bending to small radius of curvature. It indicates that the via is not

completely filled with silver ink. Silver thickness on flat surface is measured to be around 0.4μm. The via diameter is 1mm, and the metal interconnect line is 300μm wide. In forward bending, the via might squeeze the silver particles together causing lower resistance data, while in backward bending, the top passivation Kapton layer applies pressure to the silver particles in the via. Bending test data on via test structure shows change in resistance by less than 5%.

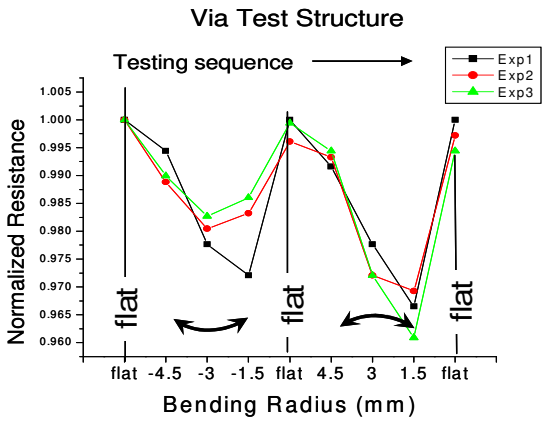


Figure 47: Bending test data for via test structure.

IV. Metal line and chain via tests

Metal line test structure is formed, as shown in Figure 48a. It consists of multiple metal lines with different lengths printed on the substrate. A second Kapton layer is capped on top with via pre-fabricated on this layer. Metal contact pads are printed in order to fill the via and connect to the underlying metal lines on the bottom substrate. Figure 48b shows a linear increase in the resistance data of metal lines as a function of

the metal line length. The results indicate that the Kapton material does not stretch during bonding and annealing processes; the vias are in the same location and provide good contact with bottom layer.

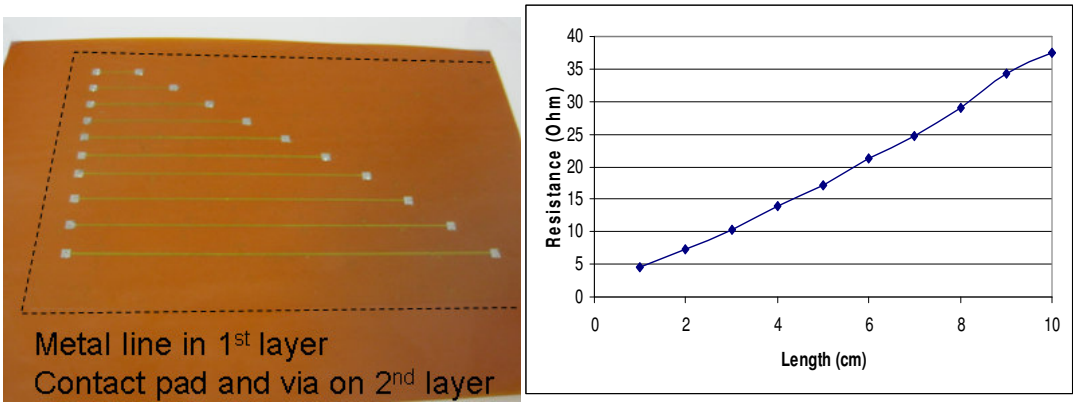


Figure 48: a) picture of metal line test structure, b) resistance measurement of metal lines at different lengths.

A Via chain test structure is also formed. In this structure, metal line is formed by multiple segments of small metal lines on top and bottom layers, connected by contact vias as shown in Figure 49. The resistance data shows that after the via chain structure is formed, the resistance between vias is higher compared to similar metal structure formed on single substrate. Another passivation layer (third Kapton film) was formed on top, and the resistance was measured again. The resistance between both ends of the via chain structure decreased as shown in Figure 49b (note that after bonding 3rd Kapton layer on the via chain structure, no access to center vias are available, excepting 2 vias at both ends). It indicates that the silver formed inside each via is porous and/or air traps within the via structure (air escapes at the open via during anneal process) are still remaining, as shown in Figure 50. As the 3rd layer is applied on the structure, the via structure is

sandwiched between 1st and 3rd Kapton layers. During the bonding anneal process of the 3rd layer, air bubbles are removed between layers due to heat and pressure keeping the silver ink powder intact.

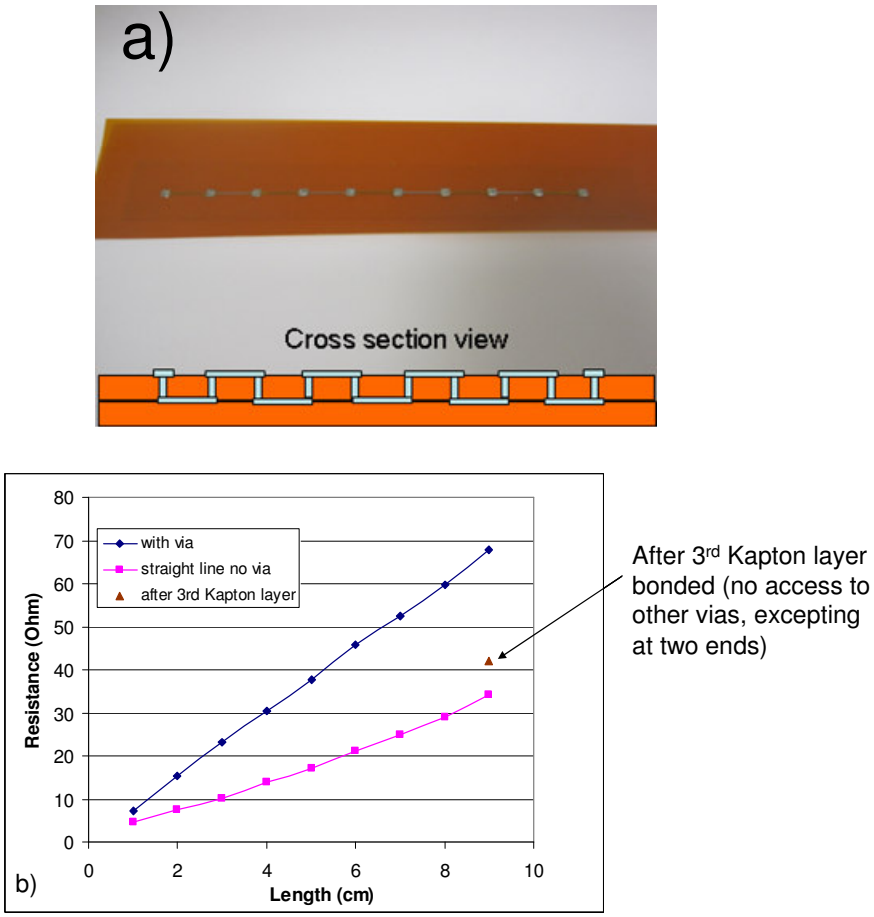


Figure 49: a) Picture and schematic cross section of the via chain test structure, b) resistance data measured at each contact via. Blue line is the measured data of the via chain test structure, purple line is measured data on same structure on single substrate, single triangle data is measured at each ends of the via chain structure after 3rd Kapton layer bonded (note that after bonding 3rd Kapton layer on the via chain structure, no access to center vias are available, excepting 2 vias at both ends).

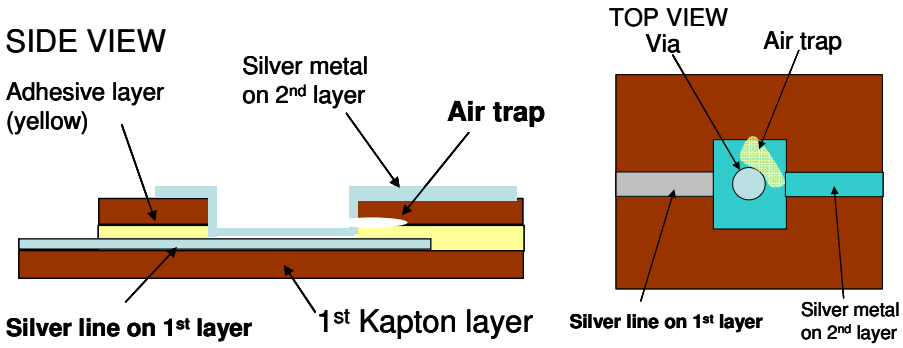


Figure 50: Cross section and top view of the via structure. Air trap present at the via could cause high resistance.

V. Multilayer metal interconnect demonstration

As a demonstration, long via chain structures, as schematically shown in Figure 51 are formed. One end of the structures is connected to power supply and the other end to a light emitting diode (LED). It can be seen that a continuous metal path is formed, thus lighting up the LEDs, as shown in Figure 51. The structures show good connection even under bending.

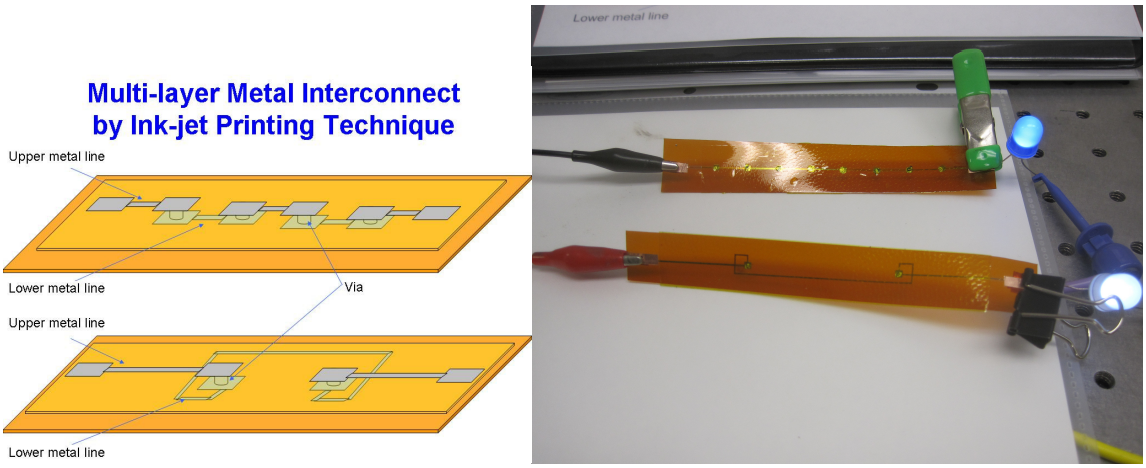


Figure 51: a) Schematic of multilayer demonstration structure; b) picture of flexible multilayer metal interconnection demonstration.

VI. Summary

A simple cost effective technique to form multilayer metal interconnection for flexible circuit has been developed. The technique utilizes inkjet printing technique to fill metal silver ink into the via. Bending test data on via test structure shows change in resistance by less than 5%.

Chapter 6: Phased-Array Antenna System

I. Introduction

Flexible antenna has become more attractive in recent times due to the development of several interesting flexible circuit components that can be integrated into one system on a light weight, conformal flexible platform. Since different communication tasks require different antenna technologies, a flexible antenna is important for several communication applications. For example, proximity surface activity applications such as on robotic devices or on human clothes, mandate a small size, light weight, and low power antenna system that can be used in a desired frequency band for certain data services. Due to the low profile of conformal antenna designs, the local networks for flexible antennas are expected to provide coverage for short (~ 10 m) to medium range (~ 5-10 km) operation [1].

A very important flexible antenna system, namely the phased array antenna (PAA), is formed by combining the flexible antenna elements and electronics involved, such as transmit/receive (T/R) modules for controlling the system, on a single flexible substrate. The PAA plays an important role in the modern radar system since it can electrically scan the beam in a wide angular range without the need for mechanically rotating the antenna [2]. However, embedding the phase shifting chip on a flexible substrate is not an easy task since the fabrication resolution limit of 50μm line widths achievable from the printing technique, and the limitation on the available flexible substrate material/design, render the size of the embedded electronics to be large. The

assembly of these components on flexible substrate; therefore, is prone to reliability issues.

In this chapter, the design, fabrication and testing of a 2-bit 1x4 phased array antenna system will be presented.

II. Phased-array antenna design

1. Design of impedance matched 5GHz patch antenna:

Figure 52 (a) shows a typical microstrip antenna, which is basically a conductor printed on top of a layer of substrate with a backing ground plan. The length is L; width is W; the dielectric thickness is h; and the material dielectric constant is ε_r. In most microstrip end fed antennas, the feed line impedance ($50\,\Omega$) is not always the same as the radiation resistance at the edge of the patch, which is usually a few hundred ohms depending on the patch dimensions and the substrate used. As a result, this input mismatch will affect the antenna performance because maximum power is not being transferred. Thus, an inset feed as in Figure 52(b) will be used to match the antenna, because the resistance varies as a cosine squared function of the inset distance x_0 [3-5].

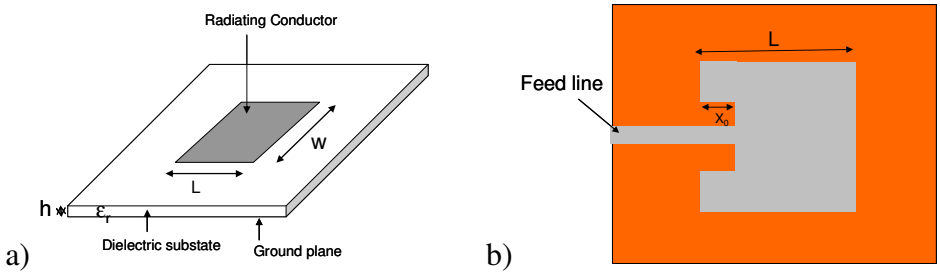


Figure 52: (a) A typical microstrip antenna, (b) an inset fed microstrip antenna.

The width and the length of the patch is made approximately $\lambda_g / 2$ (λ_g is the wavelength of the operating RF signal in the substrate). Since the dimension is designed to help maximize efficiency, the average of the value for ε_r of the substrate and ε_r of air (ε_r=1) are used to obtain a half-wavelength when designing the width W as shown in equation (1).

$$W = \frac{c}{2 f_0 \sqrt{\frac{\varepsilon_r + 1}{2}}} \tag{1}$$

The effective dielectric constant due to the air/dielectric boundary is expressed as ε_{eff}, and given by [6]:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}(1 + \frac{10h}{W})^{-1/2} \tag{2}$$

Due to the fringing fields along the radiating edges of the antenna, there is a line extension ΔL associated with the patch, which is given by [6]:

$$\Delta L = 0.412h \frac{(\varepsilon_{eff} + 0.3)(\frac{W}{h} + 0.264)}{(\varepsilon_{eff} - 0.258)(\frac{W}{h} + 0.8)} \tag{3}$$

The effective length of the antenna due to the substrate dielectric constant is given by:

$$L_{eff} = \frac{c}{2 f_0 \sqrt{\varepsilon_{eff}}} \tag{4}$$

Therefore, the design length of the microstrip antenna will be the effective length minus the line extension on both edges, which is expressed as

$$L = L_{eff} - 2\Delta L \tag{5}$$

The analysis of the inset fed distance is summarized in [4,5] which uses a transmission line network model to analyze the antenna as in Figure 53.

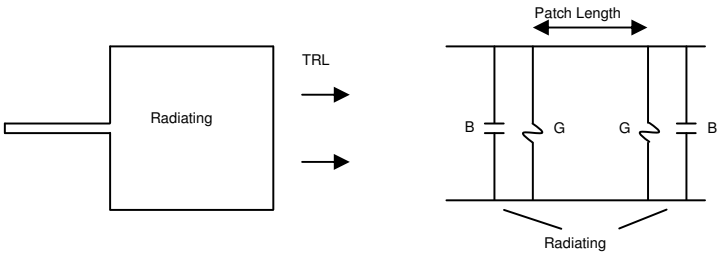


Figure 53: Transmission line network model of a rectangular patch antenna.

The input resistance of the antenna is expressed as

$$R_{in} = \frac{1}{2(G_1 + G_{12})} \tag{6}$$

where G_1 is self conductance, G_{12} is mutual conductance.

The self conductance can be calculated using the following expressions [7]:

$$G_1 = \frac{I_1}{120\pi^2} \tag{7}$$

where I_1 is the integral defined by:

$$I_1 = \int_0^{\pi} \left[\frac{\sin(\frac{k_0 W}{2}\cos\theta)}{\cos\theta} \right]^2 \sin^3\theta d\theta \tag{8}$$

where $k_0 = 2\pi / \lambda_0$.

The mutual conductance is calculated using the following expressions [8]:

$$G_{12} = \frac{1}{120\pi^2}\int_0^{\pi}\left[\frac{\sin(\frac{k_0 W}{2}\cos\theta)}{\cos\theta}\right]^2 J_0(k_0 L\sin\theta)\sin^3\theta d\theta \qquad (9)$$

where J_0 is Bessel function of the first kind.

The input resistance for an inset fed patch is given by the simplified expression [5]:

$$R_{in}(x = x_0) = \frac{1}{2(G_1 + G_{12})}\cos^2(\frac{\pi x_0}{L}) \qquad (10)$$

where x_0 is the inset feed distance.

When x_0=0, the resistance at the edge of the patch can be found as:

$$R_{in}(x = 0) = \frac{1}{2(G_1 + G_{12})} \qquad (11)$$

The optimum value of x_0 for R_{in}=50 Ω can be found using the following expression:

$$x_0 = \frac{L}{\pi}\arccos(\sqrt{\frac{50}{R_{in}}}) \qquad (12)$$

An inset feed patch antenna is designed to work at 5GHz. The dielectric material is Kapton polyimide with 100 μm thickness and dielectric constant of 2.16. The designed patch antenna parameters are W = 2.41cm, L = 2.05cm, X_0 = 7.2mm.

2. Design of microstrip transmission line:

Typical microstrip transmission line is used to provide phase shift as illustrated in Figure 54. ε_r is the relative dielectric constant of substrate, W is the width of transmission line, t is the thickness of the strip line, and h is the thickness of the substrate.

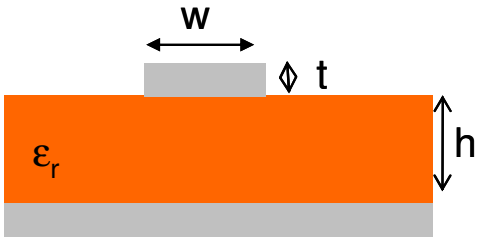


Figure 54: Microstrip transmission line.

The effective dielectric constant due to the air/dielectric boundary is expressed as ε_{eff} and given by [9]:

$$\text{For } \frac{W}{h} < 1 \qquad \varepsilon_{eff} = \frac{\varepsilon_r + 1.0}{2} + \frac{\varepsilon_r - 1.0}{2}\left[\frac{1}{\sqrt{1+\frac{12h}{W}}} + 0.04\left(1-\frac{W}{h}\right)^2\right] \tag{13}$$

$$\text{Else} \qquad \varepsilon_{eff} = \frac{\varepsilon_r + 1.0}{2} + \frac{\varepsilon_r - 1.0}{2}\left[\frac{1}{\sqrt{1+\frac{12h}{W}}}\right]$$

The characteristic impedance (Z_o) of a microstrip transmission line can be calculated using the following expression [9]:

$$Z_0 = \frac{120\pi}{2.0\sqrt{2.0\pi}\sqrt{\varepsilon_r + 1.0}} \ln\left\{1.0 + \frac{4.0h}{W'}\left[\frac{14.0 + 8.0/\varepsilon_{eff}}{11.0}\frac{4.0h}{W'} + \sqrt{\left(\frac{14.0 + 8.0/\varepsilon_{eff}}{11.0}\right)^2 + \left(\frac{4.0h}{W'}\right)^2} + \frac{1.0 + 1.0/\varepsilon_{eff}}{2.0}\pi^2\right]\right\} \tag{14}$$

$$W' = W + \Delta W'$$

$$\Delta W' = \Delta W \left(\frac{1.0 + 1.0/\varepsilon_{eff}}{2.0} \right)$$

where

$$\Delta W = \frac{t}{\pi} \ln \left[\frac{4e}{\left(\frac{t}{h}\right)^2 + \left(\frac{1/\pi}{w/t + 1.1}\right)^2} \right]$$

3. Design of co-planar waveguide coupling and transition to microstrip transmission line

For easy probing of the input RF signal at 5GHz, a grounded co-planar waveguide as in Figure 55 is designed so that both the signal and ground are on the top surface of the printed phased-array antenna system. ε_r is the relative dielectric constant of substrate, W is the width of gap, S is the width of track, and h is the thickness of the substrate.

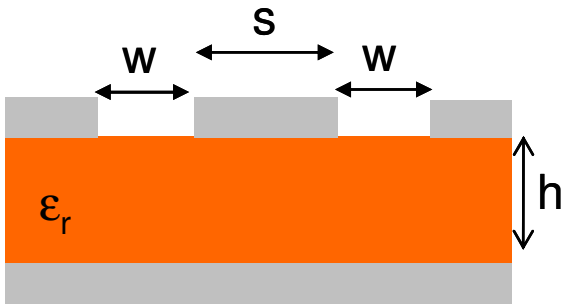


Figure 55: Co-planar waveguide transmission.

The characteristic impedance (Zo) of the grounded coplanar waveguide can be calculated as [9]:

$$Z_0 = \frac{60.0\pi}{\sqrt{\varepsilon_{eff}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(kl)}{K(kl')}} \qquad (15)$$

where $k = a/b$

$$k' = \sqrt{1.0 - k^2}$$

$$kl' = \sqrt{1.0 - kl^2}$$

$$kl = \frac{\tanh\left(\frac{\pi a}{4.0h}\right)}{\tanh\left(\frac{\pi b}{4.0h}\right)}$$

$$\varepsilon_{eff} = \frac{1.0 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(kl)}{K(kl')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(kl)}{K(kl')}}$$

The pattern of the designed co-planar waveguide for couple in RF signal is shown in Figure 56. The big pads of signal and grounds are for the ease of probing.

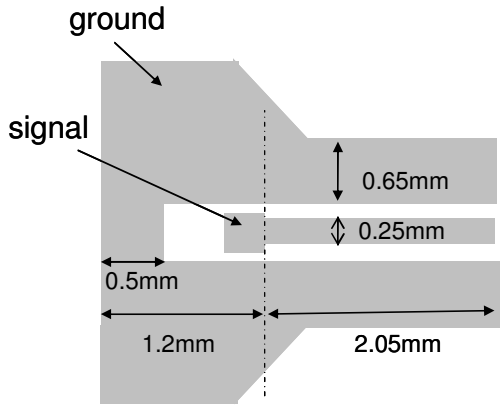


Figure 56: The designed pattern of co-planar waveguide probing

In order to make the most compact circuit, microstrip transmission lines, described in Section 1.2, are used to carry signals on the flexible substrate. Therefore, after the RF signal is carried on the co-planar waveguide, a transition section is designed to convert co-planar waveguide to microstrip line. This structure can be analyzed as a six-

port network with a ground plane, or three coupled microstrip lines [10]. The designed pattern of the transition is in the middle part of Figure 57. The coupling region is chosen to be $L=\lambda_g/4$, where λ_g is the guided wavelength of the three-conductor line [11].

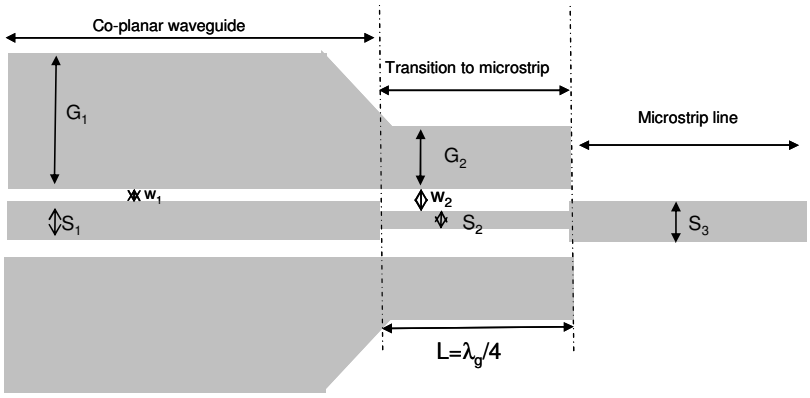


Figure 57: Co-planar waveguide to microstrip line transition.

III. Fabrication

In Chapters 2 and 4, fabrication of CNT TFT using ink-jet printing technique is discussed. In this section, the additional steps allowing CNT-TFT to be embedded to the PAA system is discussed. Figure 58 shows a schematic of the process flow for embedded CNT-TFT into PAA system. At first, the silver gate electrode is printed together with the silver transmission lines and antenna elements by utilizing Silver nanoparticle ink from Cabot Corp. After annealing the printed lines at 160^{o}C for 10 minutes, a spin-on glass dielectric material is printed on top of the gate electrode and annealed. Then, the silver source and drain (same width as transmission line which is 300 μm) electrodes are printed with the gate length of 100μm. After annealing, wet silver droplets are printed on the source drain areas to provide a good contact between source drain electrodes with

CNT film, which is captured by a special thin Kapton layer with adhesive on one side. The CNT is aligned by using dip-coat technique on sacrificial silicon substrate as discussed in Chapter 2.

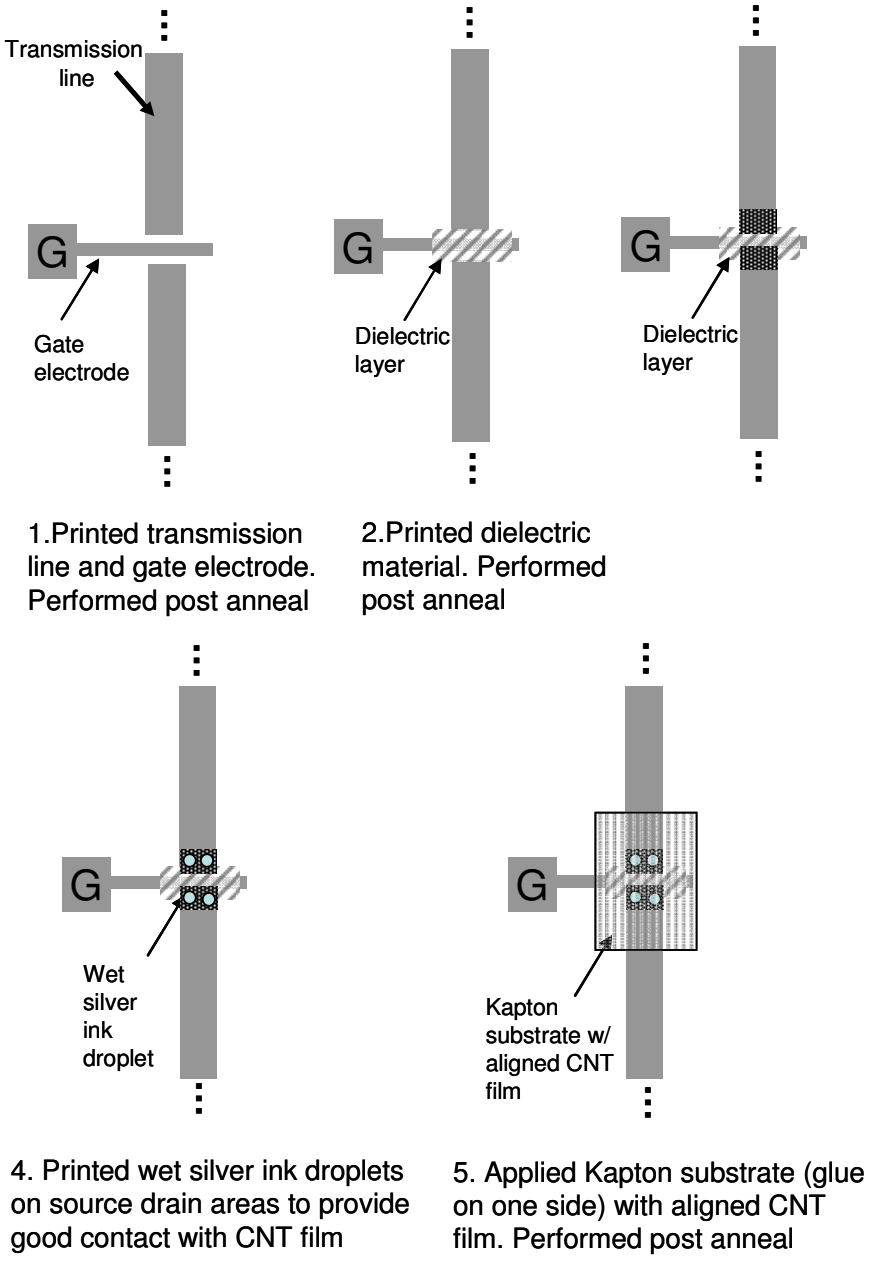
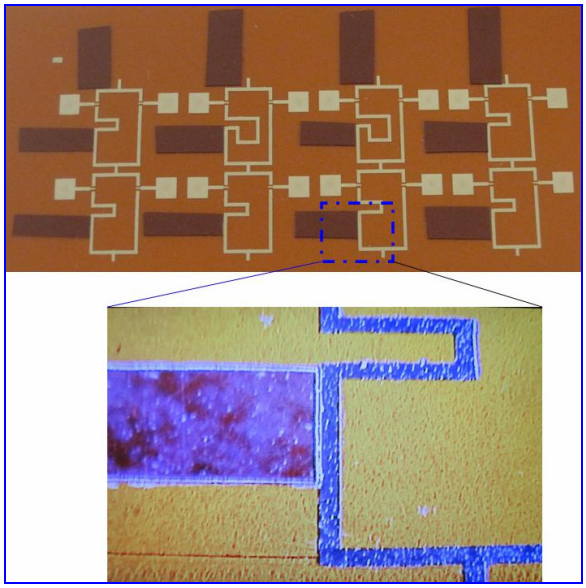


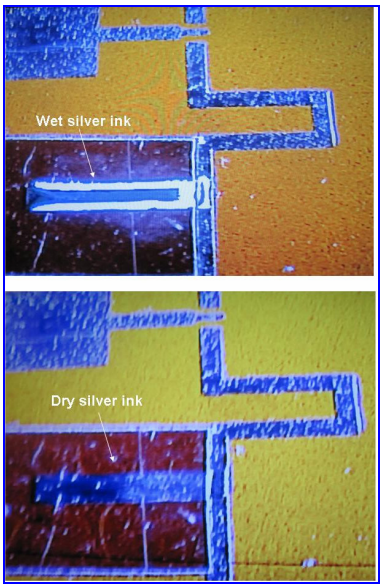
Figure 58: Schematic of bottom gate integration for our CNT-TFT which acts as a switch for the phased shifter.

Technique to test embedded CNT TFT on PAA system:

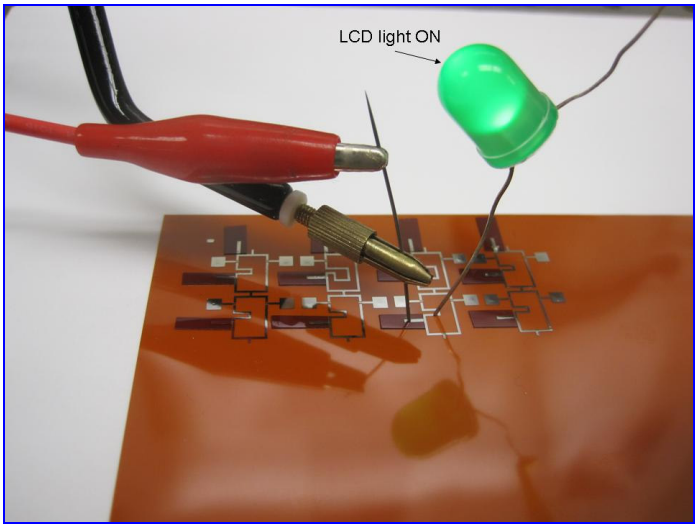
After embedding CNT-TFT on the PAA system, probing the transistor to assure it is a working device is not an easy task. If the transmission lines (for source and drain contacts) are used to test the transistor, there is a potential problem of probing needles scratching and damaging the transmission lines. A technique to form additional contact pads without changing the size and shape of the transmission line has been developed. Figure 59 shows step by step pictures of the technique. At first, a small thick Kapton film (125μm) with adhesive coating on one side is carefully taped next to the transmission line near to the CNT TFT, as shown in Figure 59a. Silver ink is printed on the top to provide the contact pad for the transistor. Figure 59b shows picture of wet and dry silver ink contacts formed on the small Kapton film. Notice that the ink is also deposited on the transmission line. Figure 59c shows the testing results, which indicate that the new contact pad does connect to the transmission line as the LCD light turns ON. After the CNT TFTs are tested, these small Kapton strips can be removed from the circuit without changing the shape of the transmission lines or leaving any damage behind as shown in Figure 59d.



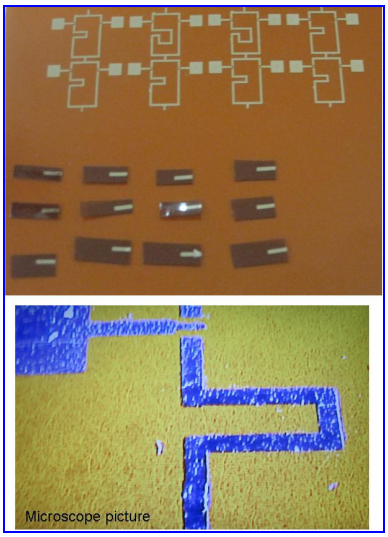
a) Applying strips of Kapton film next to transmission line



b) Print contact on the strip



c) Annealing and testing the CNT TFT



d) Taking off the strip

Figure 59: Process flow describes the technique of forming contact pads to test for embedded CNT TFT in the PAA system.

IV. Design of a 2-bit, 1x4 PAA system

Using the design method discussed above, a 2-bit 1x4 PAA system has been designed and fabricated. Figure 60 shows the layout of the 2-bit, 1x4 element phased array antenna subsystem. First, the RF signal is applied through the RF input coupling section. This coupling section transitions the signal from the coplanar waveguides to the microstrip line. The signal is then split into two branches, with each branch split further into two more branches, thus giving 4 branches with equal length (for 4 elements). Each of the 4 branches feed a phase shifting network, that controls the phase of the RF signal, via controlling the ON/OFF states of the CNT TFTs. The signals from the phase shifters feed the antenna elements.

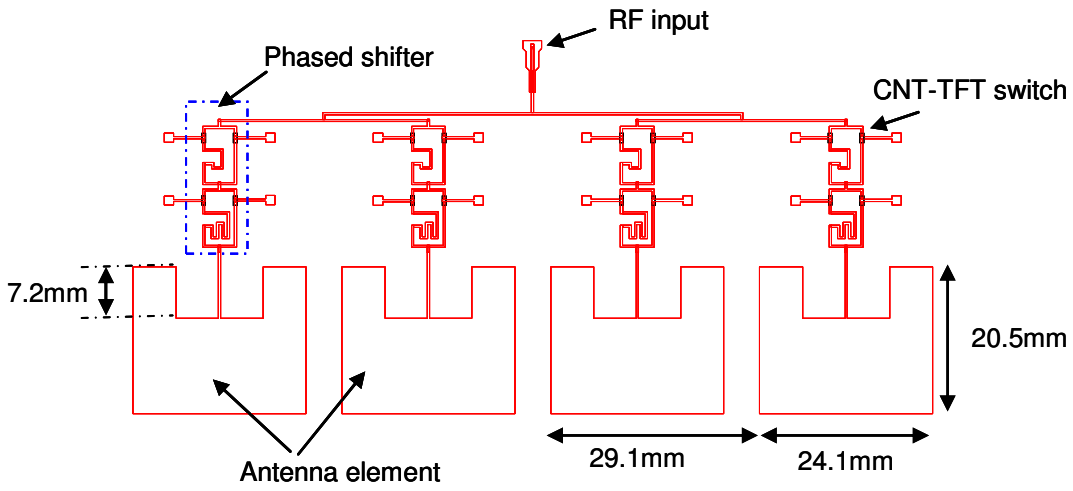


Figure 60: Schematic design of a 2-bit, 1x4 Phased-Array Antenna.

A block diagram of the 2-bit phase shifter is shown in Figure 61. Each of the switches in the phase shifter is a CNT-TFT.

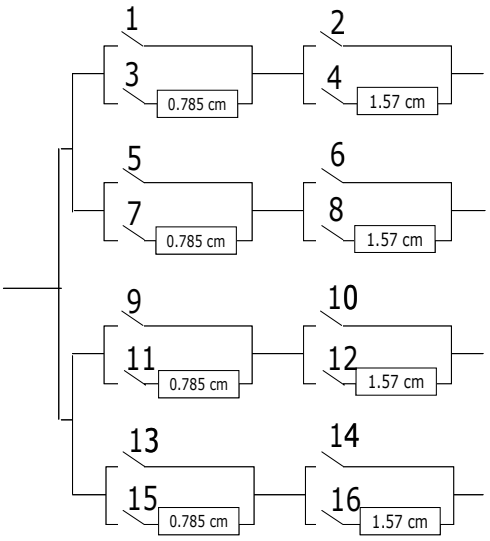


Figure 61: 2-bit, 1x4 array phase shifter design.

Table 6 shows the switching pair selection for the phase shifter versus steering angle for the designed PAA system. Switch numbers are shown on Figure 61. By controlling the ON/OFF states of the switch pairs, as indicated in Table 6, beam steering at -27 ^{o}, 0 ^{o}, 27 ^{o}, and 45^{o} is achieved. This PAA system is designed for operation at 5GHz (C-band).

Switch Pair Selection	Length difference between adjacent elements	Steering Angle
1, 2 6, 7 9, 12 15, 16	0.785cm	27º
3, 4 5, 8 10, 11 13, 14	-0.785cm	-27º
1, 2 5, 6 9, 10 13, 14	0	0º
1, 2 5, 7	2.355cm	45º

Table 6: Switching selection versus steering angle for 2-bit, 1x4 PAA system.

IV. Multilayer Metal Interconnection

Multilayer metal interconnect is also developed to provide connection to the gate electrodes from an external power supply. Chapter 5 describes the integration in detail about multilayer metal interconnect. In this section, a brief overview about the integration to form a complete PAA system is discussed. A thin Kapton (25μm) substrate with adhesive coating on one side is bonded on top of the first substrate containing the printed PAA subsystem. Contact vias are formed prior to attaching in order to obtain metal contacts with the gate contact pads on the first substrate. A pressurized annealing process on a heat chuck at 100^{o}C is used to bond these layers together. Then, silver ink is printed on the top layer to form the metal connection lines. The liquid silver ink is printed one or multiple times to fill the contact vias, which makes contact between the bottom gate contact pads and top interconnection lines. Another anneal process is performed in order

to evaporate the remaining solvent in the silver solution to form solid silver filled contact vias. Figure 62 shows a picture of a fabricated 2-bit, 1x4 PAA system on a Kapton substrate. Notice that a third thin Kapton layer is applied on top of the second layer to protect the metal interconnection lines and vias. Probing pads are formed using double-sided copper tape.

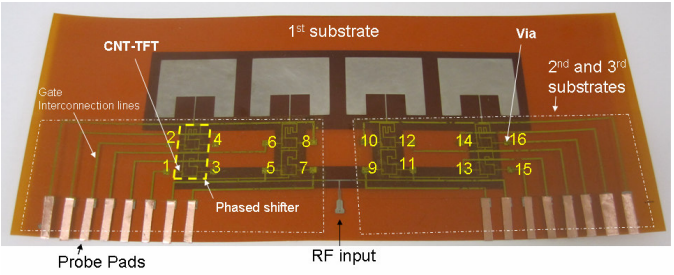


Figure 62: Picture of a complete 2-bit 1x4 PAA system containing CNT-TFTs as switches in the phase shifting network. Multilayer metal interconnection produces a fully packaged system with metal interconnection lines.

V. Experimental set up and data

The S_{11} parameter of the printed thin film antenna is measured first to confirm the radiation of the patch antenna, as shown in Figure 63. It can be seen from the figure that the antenna radiates well around 5.3GHz.

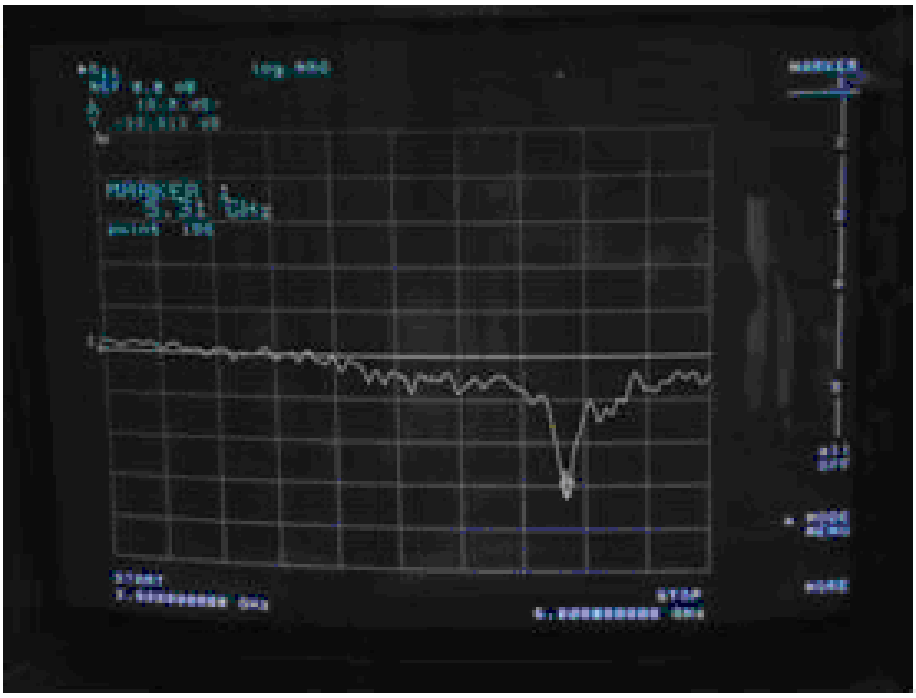


Figure 63: S11 parameter of the 1x4 PAA system.

The next step is to measure the PAA far-field pattern. Figures 64 (a) and (b) show the entire measurement setup with the network analyzer, receiving horn and microwave spectrum analyzer (MSA). The RF signal from a HP8510C network analyzer is applied at the input of the PAA system. The PAA system is spread out flat on a thick flexi glass substrate. The stage is built on flexi glass so it can also be used to perform bending experiments and study the influence of bending on far-field patterns. The entire circuit is mounted vertically on a precision rotation stage along with the DC and RF probes. The CNT-TFT switch network is controlled using a mainframe computer with a switch control module. As shown in Table 6, for each steering angle, 8 CNT-TFT switches are controlled corresponding to each desired steering angle. RF absorbers are arranged around the PAA setup in order to eliminate multi-path effects. The radiated signal is

received by a receiving horn antenna which is connected to a microwave spectrum analyzer (MSA). The received power is measured on the MSA as a function of the rotation angle, thus producing the far field patterns.

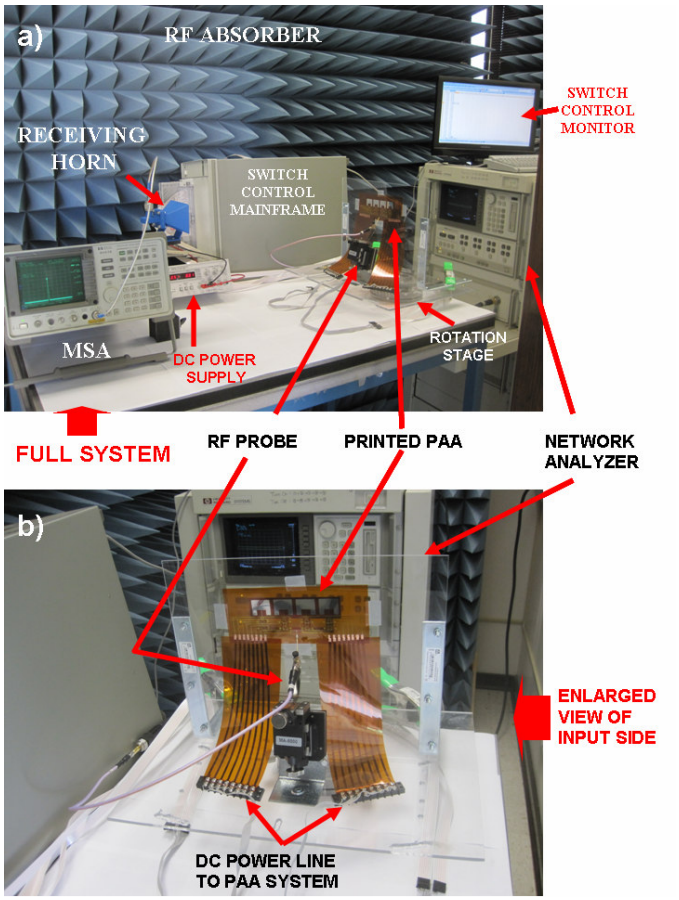


Figure 64: a) Experimental setup to measure the far-field radiation pattern of the printed 1x4 PAA system, b) Close up picture showing the 1x4 PAA system laid flat on a flexi-glass substrate holder.

The radiation pattern for a 5.3GHz signal is collected using the above. All the four azimuth steering angles are measured. Figure 65 shows the measured and simulated far

field radiation patterns of the PAA system at 0 degree (black curves) and -27 degree (red curves) steering angles. The measured points are indicated by data points whereas the simulated patterns are shown as smooth curves. It can be seen from the results that the measured and simulated far field patterns agree very well with each other.

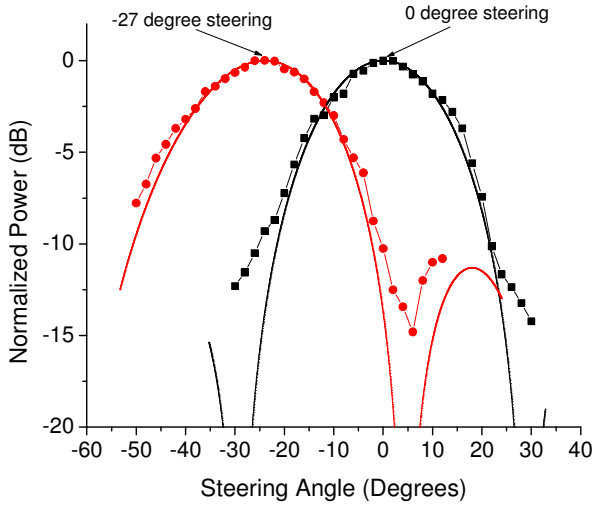


Figure 65: Measured and Simulated Far-Field Radiation Patterns of the Printed PAA system for 5.31GHz signal at 0 degree (indicated by black curves) and -27 degrees (indicated by red curves).

The efficiency the 2-bit 1x4 PAA system is calculated to be 42% including the loss of transmission line, FET switch, and coupling loss of RF probes.

VI. Bending experiment

Bending experiment is performed to observe the effect of bending on the far-field radiation pattern of the PAA system. Three PAA samples were fabricated to evaluate their bending characteristics. The PAA system is spread out on circular tube or on bent flexi glass substrate. The entire measuring setup is similar to that shown in Figure 21.

In order to evaluate the effect of bending on far-field radiation pattern, simulation code is developed to simulate the far-field radiation of the PAA patterns. The code is shown in Appendix C. Figure 66 shows the measured (indicated by data points) and simulated (indicated by smooth curves) far-field radiation patterns for four different bending radii.

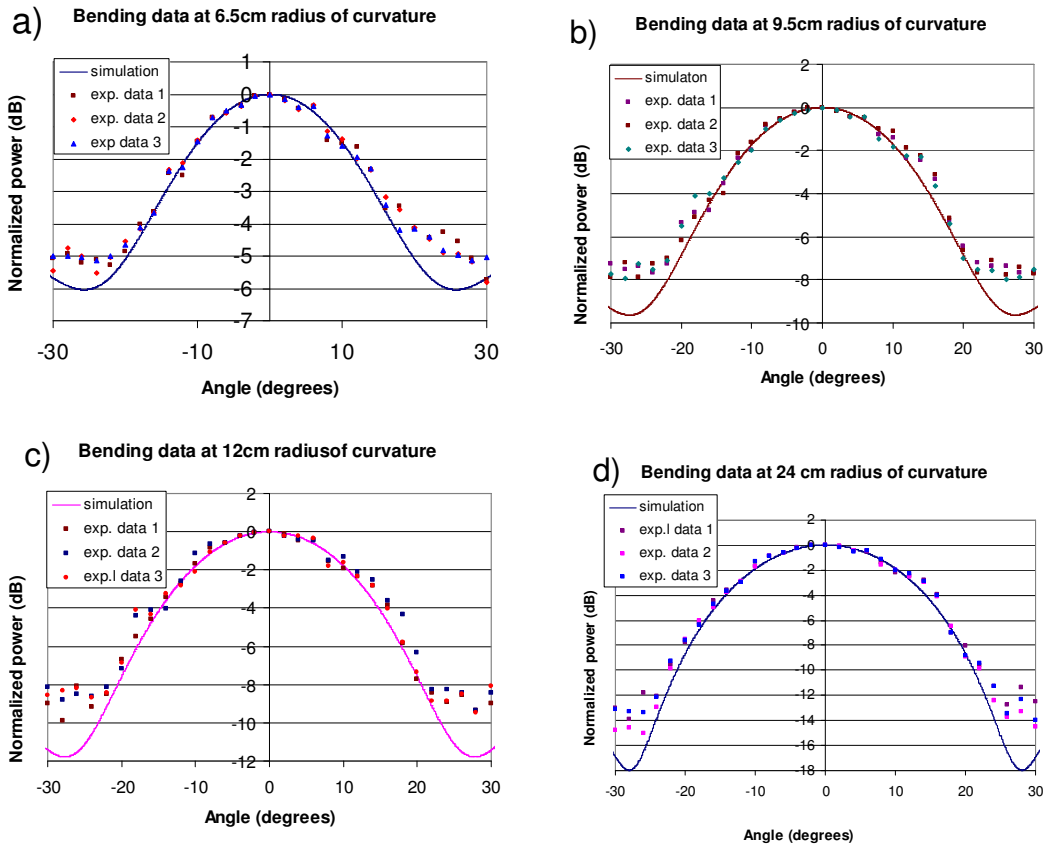


Figure 66: Theoretical (solid) and measured (dots) far-field radiation pattern for (a) 6.5cm bending radius, (b) 9.5cm bending radius, 12cm bending radius, and (d) 24cm bending radius.

A summary plot showing the calculated and measured θ_{3dB} as a function of bending radius of curvature is shown in Figure 67 for all three PAA systems. It can be seen that the measured and calculated curves agree well with each other, thus confirming good operation for conformal operations.

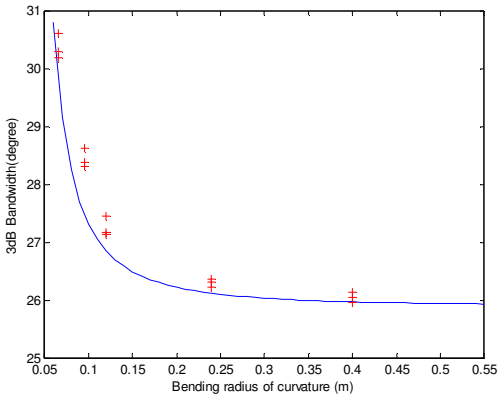


Figure 67: Theoretical (solid) and measured (crosses) 3dB bandwidth of the far-field radiation pattern as a function of bending radius of curvature.

VII. 2-Dimensional phased-array antenna

Similar to the 1x4 PAA system design, a 2-bit 2x2 PAA system has been designed and fabricated. With the 2 dimensional phased-array antenna, the beam can be steered in 2 dimensional directions and can be used in practical applications. Figure 68 shows the layout of the 2-bit, 2x2 element phased array antenna subsystem.

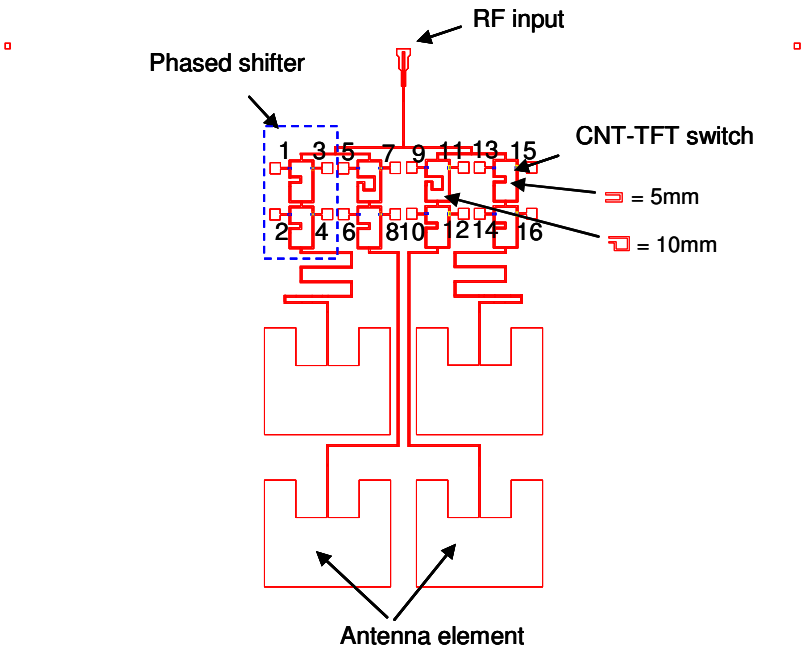


Figure 68: Schematic design of a 2-bit, 2x2 Phased-Array Antenna.

Table 7 shows the switching pair selection for the phase shifter versus steering angle for the designed PAA system. Switch numbers are shown on Figure 68.

Switching Pair Selection	Steering Angle	
	θ	ϕ
(3,4) (7,8) (15,16) (11,12)	0^o	0^o
(3,4) (7,6) (15,16) (11,10)	14.5^o	0^o
(3,4) (7,6) (15,14) (9,12)	20.7^o	45^o
(3,4) (8,5) (15,16) (9,12)	30^o	0^o
(3,4) (8,5) (15,14) (9,10)	34^o	26.5^o
(3,2) (5,6) (15,16) (9,12)	34^o	-26.5^o

Table 7: Switching selection versus steering angle for 2-bit, 2x2 PAA system.

` To measure the fair-field radiation pattern, similar measurement setup as 1-dimensional system is used; however, the 2 dimensional scan is used in this case. Figure 68 shows the entire measurement setup. Notice the receiving horn is rotated around x and y axes of the antenna.

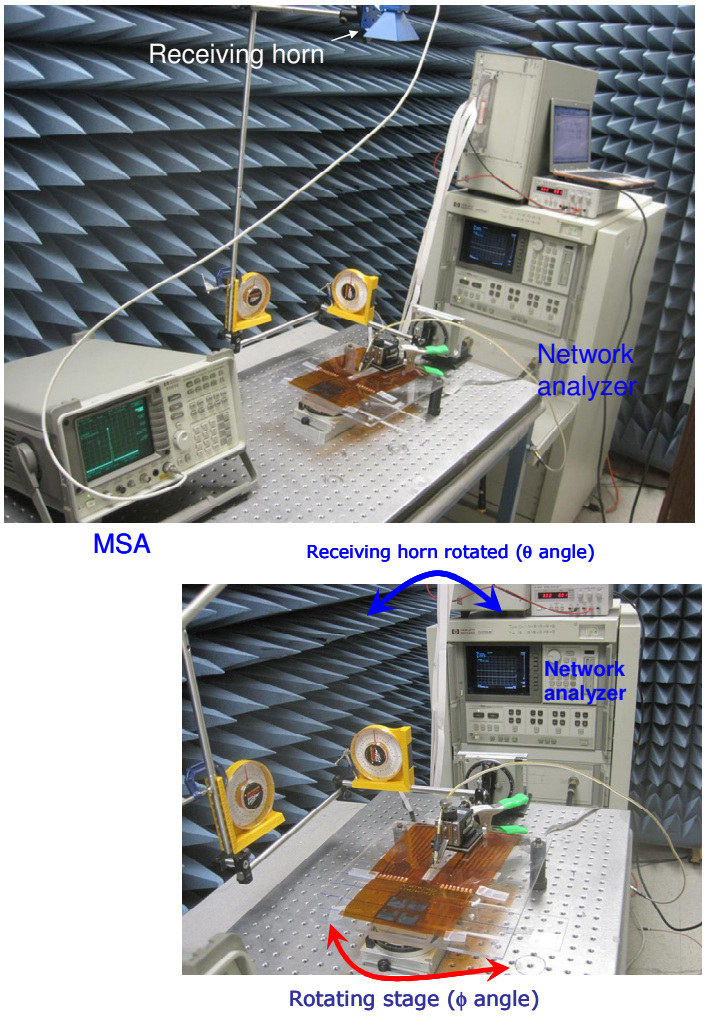


Figure 69: (top) Experimental setup to measure the far-field pattern of the printed 2x2 PAA system. (bottom) Close up picture showing the 2x2 PAA system laid flat on a flexi-glass substrate holder.

Figure 70 shows the measured far field radiation pattern of the 2x2 PAA system at different ϕ angles of 0^{o}, 45^{o} and 90^{o}. The switching pair are (3,4) (7,6) (15,14) (9,12); targeting steering angle of $\theta=20.7^{o}$ and $\phi=45^{o}$. From the measured data, the data show the peak of the pattern is located on $\phi=45^{o}$ and $\theta=20.7^{o}$ as expected.

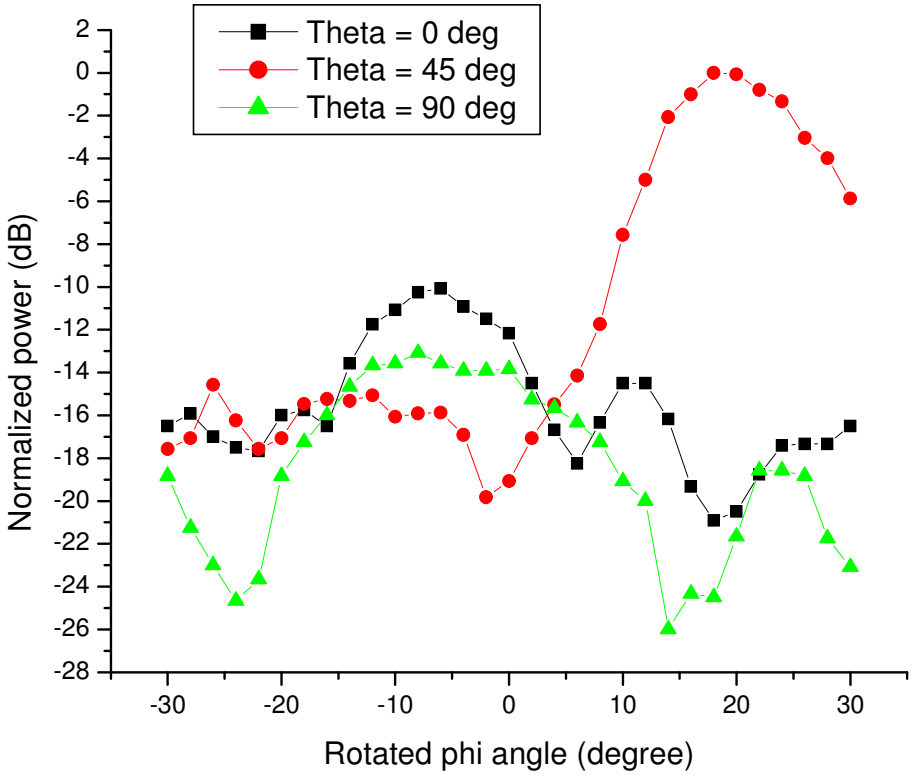


Figure 70: a) Measured far-field radiation pattern of printed 2x2 PAA system rotated. The PAA system setup for beam steering angle of θ=20.7^{o} and ϕ=45^{o}.

The efficiency the 2-bit 2x2 PAA system is calculated to be 46% including the loss of transmission line, FET switch, and coupling loss of RF probes.

VIII. Simulation codes

Appendix B: Simulation code for far-field radiation of 1x4 PAA system.

Appendix D: Simulation code for far-field radiation for bending 1x4 PAA system.

Appendix B: Calculation code for transmission line and antenna element design.

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Chapter 7: Conclusions and Future Directions

I. Conclusions and future directions for carbon nanotube thin-film transistor

Carbon nanotube thin-film transistors on flexible substrate have been fabricated in this work. Several key solutions have been developed to solve the fabrication problems. These developments relax strong constraints for flexible electronics, providing an open route for realistic applications using self-aligned CNT-TFTs and multilayer metal interconnection for flexible electronics technology. The key developments are:

- A novel source-drain contact technique is developed to provide better contact between source drain metal electrodes and CNT channel. In this technique, droplets of silver ink are printed on the source and drain areas on the first substrate prior to the application of the CNT thin-film. These wet silver ink droplets allow the silver liquid to "wet" the CNT thin-film area and enable good contact with the printed source and drain contact after annealing. This technique allows the bottom gate integration technique (or CNT channel last) to be used.

- A passivation layer to protect the device channel is also developed by bonding thin Kapton substrate on top of the device channel. This thin Kapton layer is also used as a transferring media for aligned CNT thin-film on the device substrate. Using this technique, printing dielectric material for passivation can be avoided, thus preventing inter-diffusion of dielectric material into the CNT film.

- The device structure such as gate, source, and drain electrodes and dielectric layers are printed by ink-jet printing while the CNT thin-film is transferred to the device substrate by a stamping technique. The CNT channel is an aligned CNT thin-film formed by using a new modified dip-coat technique. This novel modified dip-coat technique utilizes the capillary effect of a liquid solution rising between gaps to coat a CNT solution on large area of the substrate while using minimal CNT solution.

- Similar to silicon semiconductor devices, flexible electronics also require multiple layers and interconnections for its circuits in order to be useful for future applications. In this work, a simple and cost effective technique to form multiple layers of metal interconnection on flexible substrates has been developed and demonstrated. Contact vias are formed on the second substrate prior to bonding on the first substrate. An ink-jet printing technique is also used to fill silver ink into the via structure. The printed silver ink penetrates through the vias to contact with the contact pads on the bottom layer.

The results: High drain current of 0.476mA was obtained at V_G= -3V and a source-drain voltage (V_{DS}) of -1.5V. Bending tests performed on CNT TFT showed less than 10% variation in the performance. Bending test was also performed on via structures, which yielded less than a 5% change in resistance

Future Directions:

At the current stage, semiconducting CNT material of only 99% purity is available. Higher purity semiconducting material is needed for better device performance. Also, better dielectric ink material is needed with better surface properties, allowing other materials to be printed on for device scaling purposes. A new dielectric material for use as a passivation layer is required to reduce the topography currently required when using thin Kapton film as the passivation layer. This new passivation material is required to have less diffusion into the porous CNT thin film. By reducing the device topography, multiple circuit layers can be formed.

II. Conclusions and future directions for phased-array antenna

Compared to traditional antenna design, the antenna systems designed in this work are light weight, flexible, conformal, and can be formed entirely on a flexible substrate utilizing a room temperature, low cost ink-jet printing technique. These PAA systems are good candidates for portable wireless systems to meet challenging requirements. In this work, four elements in 1-dimensional and 2-dimensional phased-array antenna systems have been designed and fabricated. A multilayer metal interconnection scheme is used to make a complete PAA system with control lines. The phase shifting network utilizes CNT TFT as a switching element. In a 1-dimensional PAA system, by controlling the ON/OFF states of the transistors, beam steering of a 5.31GHz signal from 0^o to -27^o has been demonstrated. The antenna system also shows

good stability and tolerance under different bending radii of curvature. A similar demonstration has been conducted for a 2-dimensional PAA system. Two dimensional beam steering of a 5.2GHz signal at an angle of $\theta=20.7^{o}$ and $\phi=45^{o}$ has been demonstrated. The total efficiency of 1-dimensional and 2-dimensional PAA systems are 42% and 46%, respectively.

Future Directions:

In this research, only bending tests have been performed on the 1-dimensional PAA system. Harsh environment testing such as low to high temperatures and contact with different chemical substances is needed. To perform these tests, a temperature and chemical environment testing chamber is required.

Even though the PAA system is flexible and can be conformal on any surface, scaling the size is also needed by finding a higher dielectric constant substrate in order to integrate a large number of elements in a given area.

Appendix A: CNT TFT Simulation

I. Introduction

Carbon nanotube thin film transistor based on network of single-walled carbon nanotube has been simulated for understanding, controlling and designing the CNT thin film suitable for TFT. Currently, available CNT TFT simulation uses a 'stick" percolation – a 2D percolating random network of nanotubes/nanowires in a rectangular domain. In that model, straight "sticks", which are presented for CNT, are randomly dispersed in the rectangular domain. Rotation angle θ is used to present the random alignment of the CNTs. This simulation does not present the true shape of CNTs (not straight but rather bending) [1-3]. At first in reference [1], for CNTs having a length of 1μm, the transport in CNT is considered as in ballistic limit. For the CNTs exceeding 1μm, diffusion limit is assumed. In the results, analytical and computed data are compared. In the second reference [2], drift-diffusion theory is used for the simulation. The data is compared only with experimental data of CNT transistor with very low CNT density 1-17/μm^2. In the third reference [3], all simulation and experimental data are normalized. The results are compared and they agree well with multiple CNT concentrations. Figure 73 shows the schematic of stick simulation used in these publications.

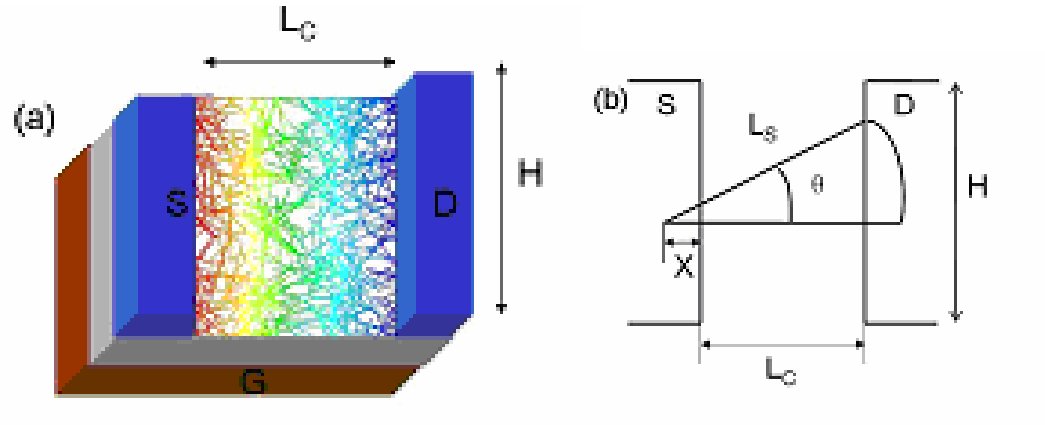

Figure 71: (a) A thin-film network transistor with channel length LC, channel width H, and individual tube length LS. Source (S), drain (D), and gate (G) are also indicated; the color code of the network reflects the typical potential distribution in a nanotube nanotube network for a channel with L_C =3μm, H=4μm, L_S = 2μm, c_{ij} =5:0, and ρ=3.5μm^{-2}. (b) Nomenclature for bridging tube calculation. (Image taken from ref [1])

II. Simulation development for carbon nanotube thin film transistor

Learning from other works, in this research, a simulation scheme using a matrix to present the CNT network using straight and random L shape for CNTs has been developed. Bent shape represents a closer model to the real shape of CNTs rather than "stick" model (Figure 74). For random CNT network, all possible shapes of straight or L shapes are introduced randomly, as shown in Figure 74, (5 shapes in all). While for the aligned CNT network, straight line and limited L shapes in the same alignment direction are introduced, as shown in Figures 74.a and 74.b. Notice that simple CNT structure formed by 5 matrix elements are shown in Figure 4.2 for demonstration purpose.

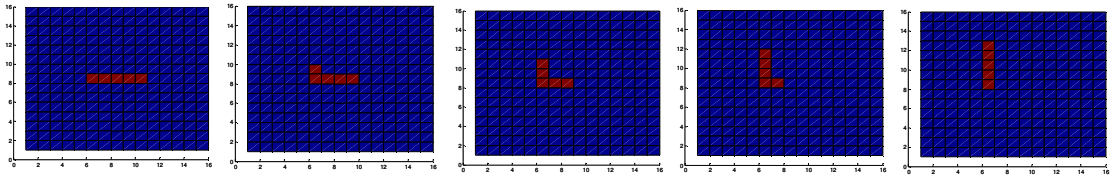

Figure 72: Shapes of CNTs used in our simulation

Using a matrix to present a CNT channel, each node (row in the matrix) is considered as a starting point for each conducting path. Each conducting path is a summation of multiple parallel paths between the source and drain electrodes. It is found that the long zig-zag path is diverted quickly (since 1/R), and it is also found that one adjacent row (top or bottom) is sufficient to present the conducting path of each node. Figure 75 describes the conducting path starting from each node.

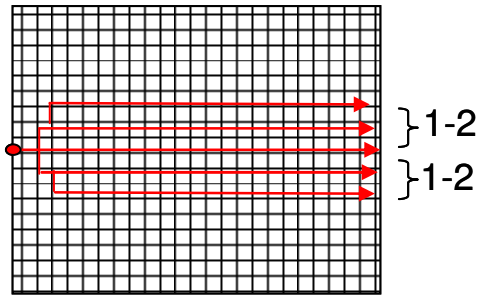

Figure 73: Conducting path model starting at each node (row) in the matrix.

To confirm the simulation, the simulation data is compared with experimental and simulation data reported in literature [3], and it shows good agreement as shown in Figure 76.

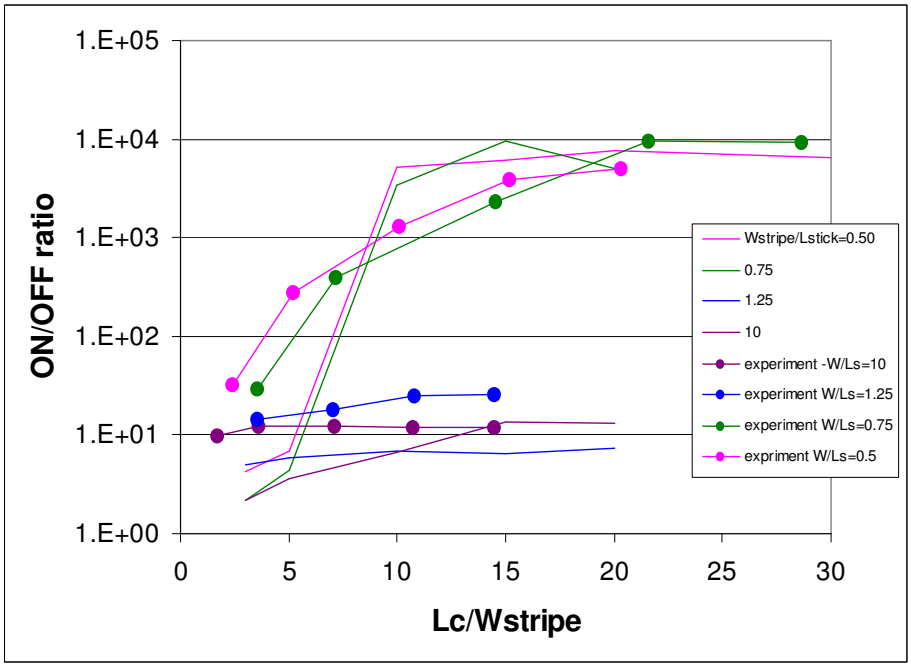

Figure 74: Comparison of our simulation results with data presented in reference [3]. Curves without data points are simulation results using our CNT L shape simulation. Curves with dots represent experimental data from [3].

III. Simulation results

The simulation code is used to predict and confirm experimental data from this research. Following are some simulation results

1. Simulation result for CNT TFT with different channel length

Simulation conditions: CNT density = 30/μm^2, Semiconducting CNT: metallic CNT = 99:1, Channel width = 300μm, CNT length = 1μm. Figure 77.a shows the simulation results using simulation code developed from this work. "NanoNet", a

simulation tool for thin film transistors based on network of nanotubes or nanowires, from *nanohub.org* is also used. The results are shown in Figure 77.b. Due to the simulation limitation (on-line), channel width of 10µm and small channel length are simulated. From both results, it can be seen that as the channel length is reduced, more CNT networks connect between source and drain electrodes; or in other words, more conducting paths connecting source and drain are formed, therefore, increasing the net drain current. Notice that 30/µm^2 CNT density is used for both simulation tools due to the limitation of the computing power and availability for NanoNet tool.

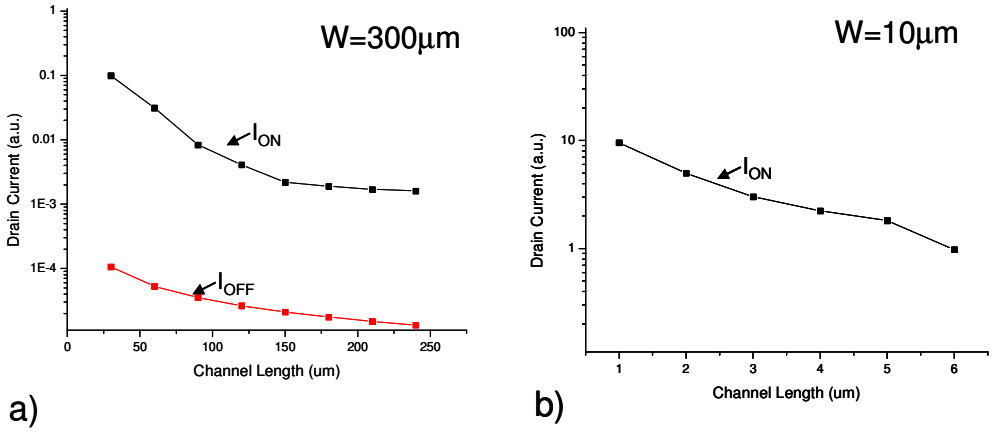

Figure 75: a) Simulation result using simulation code developed in this work, b) simulation result using NanoNet simulation tool from nanohub.org. CNT density for both results is 30/µm2.

2. Simulation result for CNT TFT with different degree of alignment

Simulation conditions: CNT density = 30/µm^2, Channel width = 300µm, Channel length = 90µm, CNT length = 1µm are used. Figure 78 shows the ON state drain current

of CNT TFT device as a function of varying degrees of CNT bending or rotating using the simulation code developed in this work. The results show that the aligned CNT thin film transistor gives higher drain current than random CNT network based transistors.

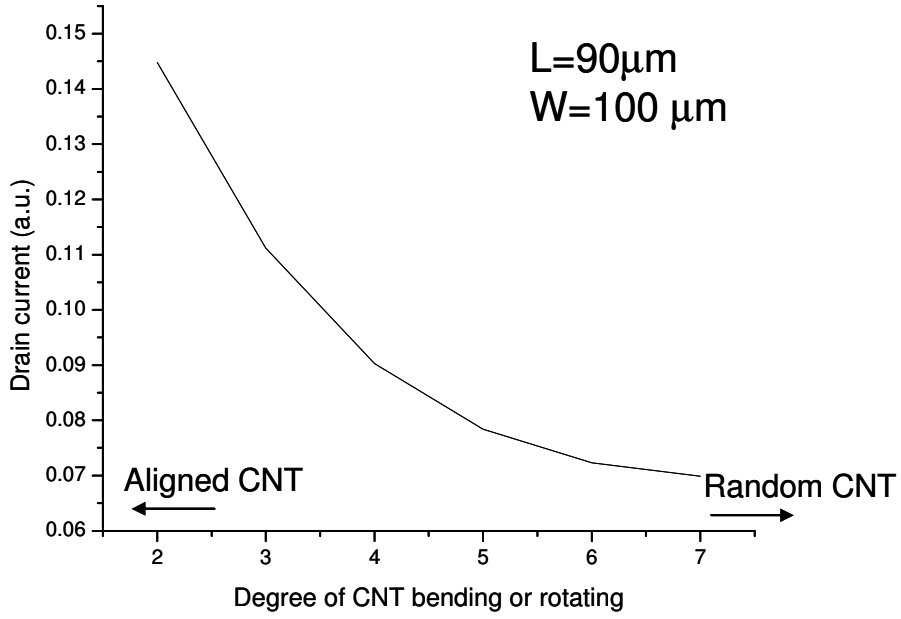

Figure 76: Simulation result of CNT TFT device with different degree of bending and rotating using the simulation code developed in this work.

In summary, simulation code has been developed for CNT TFT. The simulation result show that aligned CNT thin film provides higher drain current. Additionally, higher drain current can be obtained by scaling down the channel length.

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IV. Simulation code

```
%This Matlab code simulation CNT-thin film drain current
clear all

W=4;
L=120;
mrun=25;
srun=50;
C=ones(W,L);
C=C*100000;
countsemi=0;  %total semiconductin CNT to check at the end
countmetal=0; %total metallic CNT

%CNT is randomly introduced into matrix A which has the same size of the
%matrix presenting the CNT thin-film. Command "randerr" introduces 1
%
%L shape of the CNT is defined by random using "randint" in this program
%the CNT is devided into 7 segments.

%Calculate for ON state current
for semi=1:srun,
A=randerr(W,L,[1,2; 0.999999,0.000001]);
  for n=1:W
    for m=1:L
        if A(n,m)==1, turn = randint(1,1,[1,7]);
            C(n,m)=1;
            countsemi=countsemi+1;
            for i=1:turn,
                if n+i<W+1
                C(n+i,m)=1;
                end
            end
            for k=1:(7-turn),
                if m+k<L+1
                C(n,m+k)=1;
                end
            end
        end
    end
  end
end

for metal=1:mrun,
```

```
A=randerr(W,L,[1,2; 0.999999,0.000001]);
for x=1:W
    for y=1:L
        if A(x,y)==1, turn = randint(1,1,[1,7]);
            C(x,y)=1;
            countmetal=countmetal+1;
            for i=1:turn,
                if x+i<W+1
                C(x+i,y)=0.1;
                end
            end
            for k=1:(7-turn),
                if y+k<L+1
                C(x,y+k)=0.1;
                end
            end
        end
    end
end
end

%Current for straight line
T=sum(C');
for z=1:W,
    Ic(z)=1/T(z);
end
Iontot=sum (Ic)

%R of next row
N=C;
for h=1:W-1
    for k=1:L
        N(h, L+k)=N(h+1,k);
        P=sum(N');
        res(k)=P(h);
        cur(k)=(1/res(k));
    end
    current(h)=sum(cur);
    res=0;
    cur=0;
end
Inext=sum(current)
```

```
%Calculate for OFF state current
F=ones(W,L);
F=F*10000;
for semi=1:srun,
R=randerr(W,L,[1,2; 0.999999,0.000001]);
  for n=1:W
    for m=1:L
        if R(n,m)==1, turn = randint(1,1,[1,7]);
            F(n,m)=1;
            countsemi=countsemi+1;
            for i=1:turn,
                if n+i<W+1
                F(n+i,m)=100000;  %OFF
                end
            end
            for k=1:(7-turn),
                if m+k<L+1
                F(n,m+k)=100000;   %OFF
                end
            end
        end
    end
  end
end

for metal=1:mrun,
R=randerr(W,L,[1,2; 0.999999,0.000001]);
for x=1:W
    for y=1:L
        if R(x,y)==1, turn = randint(1,1,[1,7]);
            F(x,y)=1;
            countmetal=countmetal+1;
            for i=1:turn,
                if x+i<W+1
                F(x+i,y)=0.1;
                end
            end
            for k=1:(7-turn),
                if y+k<L+1
                F(x,y+k)=0.1;
                end
            end
        end
```

```
    end
end
end

Y=sum(F');
for z=1:W,
    Ioff(z)=1/Y(z);
end
Iofftot=sum (Ioff)
ratio=Iontot/Iofftot
```

Appendix B

Simulation code for far-field radiation pattern of 1-D PAA system

```
clear all
for j=1:1:2095
   u(j)=-pi/3+j*0.001;
end
for n=1:1:1047;
   g1(n)=(u(n)*360/(2*pi));
end
for m=1:1:1047;
   g2(m)=(u(m+1047)*360/(2*pi));
end
freq=5.49e9; %% enter frequency %
c=3e8; %speed of light %
lambda=c/freq;
d = 2.9e-2; %d between antenna in meter %
r = 100e-2; % r is the bending radius in meter %
theta =(pi/180)*(d*360)/(2*pi*r); % cal. angle
a = (pi/180)*(180-theta)/2;
y = 2*r*sin(theta/2)*sin(theta);
for k=1:1:2095
X(1,k) = 2*r*sin(theta/2)*sin(theta-u(k));
X(2,k) = 0;
X(3,k) = 2*r*sin(theta/2)*sin(u(k));
X(4,k) = sin((theta/2)+u(k))*2*r*sin(theta);
end;
for x=1:1:2095
   E(x)=0;
end
```

```
 for l= 1:1:4
   for i=1:1:2095
   Z(l,i)=cos(X(l,i)*2*pi/lambda)+sqrt(-1)*sin(X(l,i)*2*pi/lambda);
   end
 end
    for m=1:1:2095
       for n=1:1:4
       E(m)=E(m)+ (Z(n,m));
       end
    end
for n=1:1:1047;
   db1(n)=(20*log10(abs(E(n))/4));
end
for m=1:1:1047;
   db2(m)=(20*log10(abs(E(m+1047))/4));
end
    S1=interp1(db1,g1,-3);
    S2=interp1(db2,g2,-3);
    A=(u*360/(2*pi))';
    B=(20*log10(abs(E)/4))';
 %plot(u*360/(2*pi),(20*log10((abs(E)/4))),'r');
 plot(g1,db1);
   axis([-60 60 -40 0]);
   xlabel('Angle from normal of antenna (degrees)');
   ylabel('Relative Magnitude(dB)');
```

Appendix C

Simulation code for far-field radiation pattern of 1-D PAA system under bending

```
clear all
for j=1:1:2095
   u(j)=-pi/3+j*0.001;
end
for n=1:1:1047;
   g1(n)=(u(n)*360/(2*pi));
end
for m=1:1:1047;
   g2(m)=(u(m+1047)*360/(2*pi));
end
freq=5.25e9; %% enter frequency %
c=3e8; %speed of light %
lambda=c/freq;
d = 2.9e-2; %d between antenna in meter %
ra = 5e-2; % r is the bending radius in meter %
for b=1:1:50;
   r(b)=ra+(b*0.01);
theta =(pi/180)*(d*360)/(2*pi*r(b)); % cal. angle
a = (pi/180)*(180-theta)/2;
y = 2*r(b)*sin(theta/2)*sin(theta);
  for k=1:1:2095
X(1,k) = 2*r(b)*sin(theta/2)*sin(theta-u(k));
X(2,k) = 0;
X(3,k) = 2*r(b)*sin(theta/2)*sin(u(k));
X(4,k) = sin((theta/2)+u(k))*2*r(b)*sin(theta);
  end;
  for x=1:1:2095
```

```
  E(x)=0;
 end
 for l= 1:1:4
  for i=1:1:2095
  Z(l,i)=cos(X(l,i)*2*pi/lambda)+sqrt(-1)*sin(X(l,i)*2*pi/lambda);
  end
 end
 for m=1:1:2095
      for n=1:1:4
      E(m)=E(m)+ (Z(n,m));
      end
 end
 for n=1:1:1047;
  db1(n)=(20*log10(abs(E(n))/4));
 end
W=db1(1047)-3;
 for m=1:1:1047;
  db2(m)=(20*log10(abs(E(m+1047))/4));
 end
   S1(b)=interp1(db1,g1,W);
   S2(b)=2*interp1(db2,g2,W);
   E=0;
end
plot (r,S2);
hold
D=[0.065 0.065 0.065 0.095 0.095 0.095  0.12 0.12 0.12 0.24 0.24 0.24 0.4 0.4 0.4];
E=[30.18 30.61 30.29 28.38 28.63 28.31 27.14 27.44 27.17 26.36 26.22 26.30 25.95
26.13 26.05];
plot (D,E,'r+');
  xlabel('Bending radius of curvature (m)');
```

```
ylabel('3dB Bandwidth(degree)');
```

Appendix D

1-D PAA system calculation designing code

```
Clear all
% Details of design of antenna element on a dielectric substrate%
c=3e8;                                  % c is the speed of light in vacuum%
fo=5e9;                                 % fo=3GHz is the operating frequency of RF signal%
lambdao = c/fo;                         % lambdao is the operating wavelength of RF signal%
er = 2.1;                               % er is the relative permittivity =n^2%
h = 500e-6;                             % h is the height of the dielectric waveguide%
W=c/(2*fo*sqrt((er+1)/2))               % W is the width of the antenna element%
eeff = (er+1)/2 + (er-1)/2*(1+(10*h/W))^-0.5;          % eeff is the effective permittivity%
dL = (0.412*h)*(eeff+0.3)*((W/h)+0.264)/((eeff-0.258)*((W/h)+0.8));
                                        %dL is due to fringing fields%
Leff = c/(2*fo*sqrt(eeff));             % Leff is the effective length of the antenna element
taking fringing fields into account%
L = Leff-2*dL                           % L is the actual design length that needs to be
fabricated%
ko = 2*pi/lambdao;                      % ko is the free space wave number%
x=0:0.01:pi;
I1 = trapz(x,((sin(ko.*W/2.*cos(x))./cos(x)).^2).*(sin(x).^3));
I2 = trapz(x,((sin(ko.*W/2.*cos(x))./cos(x)).^2).*Besselj(0,(ko.*L.*sin(x))).*(sin(x).^3));
G1 = I1/(120*(pi^2));                   % G1 is the conductance%
G12 = I2/(120*(pi^2));                  % G12 is the mutual conductance%
Rin = 1/(2*(G1+G12));
xo = L/pi*acos(sqrt(50/Rin))            % xo is the distance into the antenna element that
the feed has to be placed%

%Details of design of microstip transmission lines on a dielectric substrate%
t = 5e-7;
```

```
e=2.71;                                  % t is the height of the transmission line%
W1 = 1.6e-3;                             % W1 is the width of the transmission line%
if W1/h<1
eff1 = (er+1)/2 + (er-1)/2*(1/sqrt(1+(12*h/W1))+ 0.04*(1-(W1/h))^2)  % eff1 is the
effective permittivity for the transmission line%
else
eff1=(er+1)/2 + (er-1)/2*(1/sqrt(1+(12*h/W1)))
end

dW = (t/pi)*log((4*e)/((t/h)^2+((1/pi)/((W1/t)+1.1))^2));
dWp=dW*((1+(1/eff1))/2);
Wp=W1+dWp;
A = (120*pi)/(2*sqrt(2)*pi*sqrt(er+1));
B = ((14+(8/eff1))/11)*(4*h/Wp);
C= sqrt(((14+(8/eff1))/11)^2+(4*h/Wp)^2 + ((1+(1/eff1))/2)*pi^2);
Zo= A*log(1+((4*h/Wp)*(B+C)))

%Details of design of transition section on a dielectric substrate%
a = 1.6e-3; % a is the width of the track%
b = a+(2*0.85e-3); %b is the spacing between adjacent ground electrodes%
k=a/b;
kp=sqrt(1-k^2);
kl = tanh(pi*a/(4*h))/tanh(pi*b/(4*h));
klp= sqrt(1-kl^2);
D=call(kp)*call(kl)/(call(k)*call(klp))
eeff2 = (1+(er*D))/(1+D)
Zo1 = 60*pi/(sqrt(eeff2)*D)
```

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